DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAC-9647
CMOS IMAGE SENSOR

648 (H) X 488 (V)
VGA 68 fps
Color CIS

September 2004
Revision 1.92

KAC-9647 Color CMOS Image Sensor VGA 68 FPS

General Description

The KAC-9647 is a high performance, low power, 1/4" VGA CMOS Active Pixel Sensor capable of capturing color, still or motion images and converting them to a digital data stream.

Great image quality is achieved by integrating a high performance analog signal processor comprising of a high speed 10 bit A/D convertor, fixed pattern noise elimination circuits and separate color gain amplifiers. The offset and black level can be automatically adjusted on chip using a full loop black level compensation circuit.

Furthermore, a programmable smart timing and control circuit allowing the user maximum flexibility in adjusting integration time, active window size, gain, frame rate. Various control, timing and power modes are also provided.

Features

- Master and slave mode operation
- Progressive scan read out with horizontal and vertical flip
- Programmable Exposure:
  - Master clock divider
  - Inter row delay
  - Inter frame delay
  - Partial frame integration
- Four channels of digitally programmable analog gain
- Full automatic servo loop for black level & offset adjustment on each gain channel
- Horizontal & vertical sub-sampling (2:1 & 4:2)
- Windowing
- Programmable pixel clock, inter-frame and inter-line delays
- I^2C compatible serial control interface
- Power on reset & power down mode

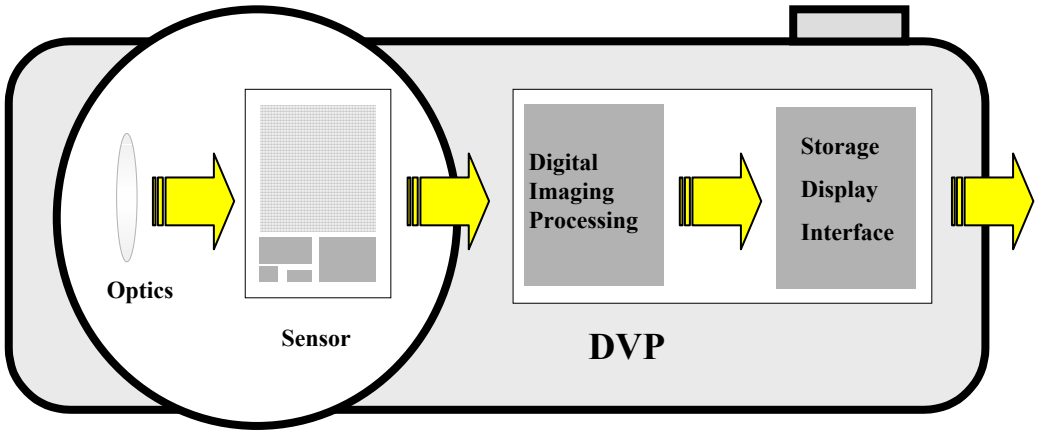
Applications

- Dual Mode Camera
- Digital Still Camera
- Security Camera
- Machine Vision

Key Specifications

Array Format	Total: 488 x 672 Active: 488(V) x 648(H)
Effective Image Area	Total: 2.93mm x 4.03mm Active: 2.93mm x 3.89mm
Optical Format	1/4"
Pixel Size	6.0µm x 6.0µm
Video Outputs	8 & 10 Bit Digital
Frame Rate	68 frames per second
Dynamic Range	57 dB
Electronic Shutter	Rolling Reset
FPN	0.2%
PRNU	1.7%
Sensitivity	2.5 volts/lux*s
Fill Factor	49%
Color Mosaic	Bayer pattern
Package	32 LCC
Single Supply	3.0V +/-10%
Power Consumption	130mW
Operating Temp	-10°C to 50°C

System Block Diagram



Overall Chip Block Diagram

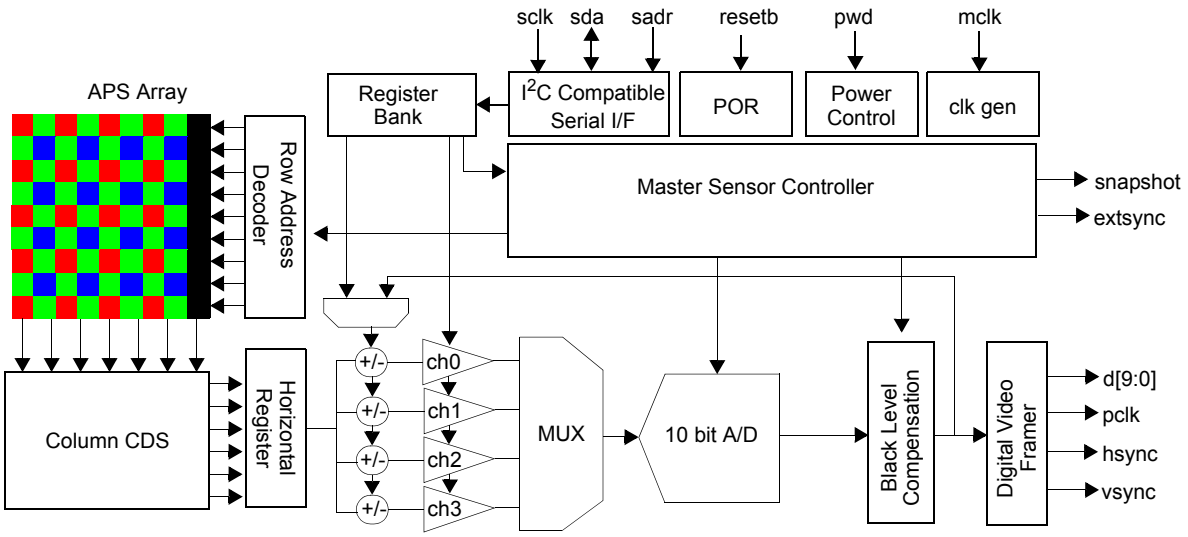


Figure 1. Chip Block Diagram

Connection Diagram

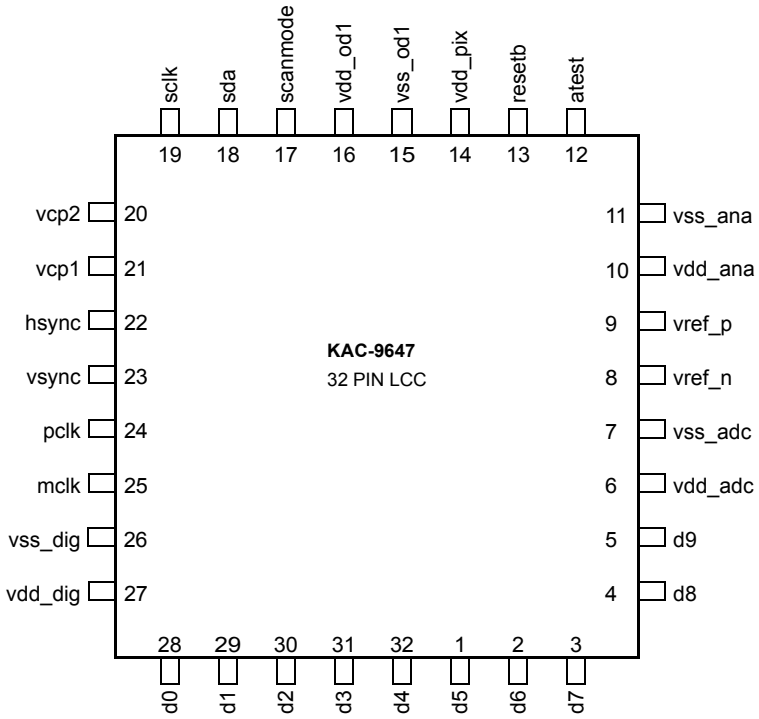


Figure 2. Chip Pin Diagram

Typical Application Circuit

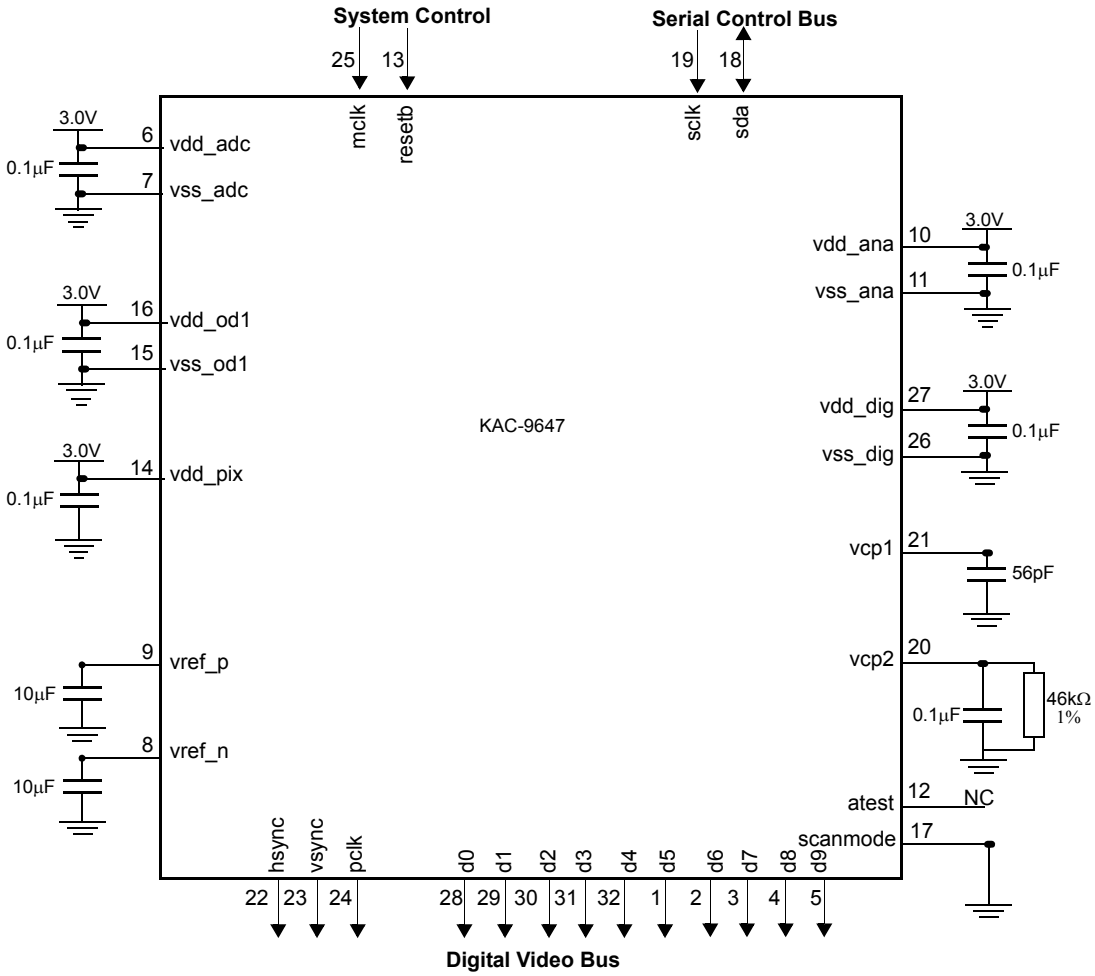


Figure 3. Typical Application Diagram

Scan Read Out Direction

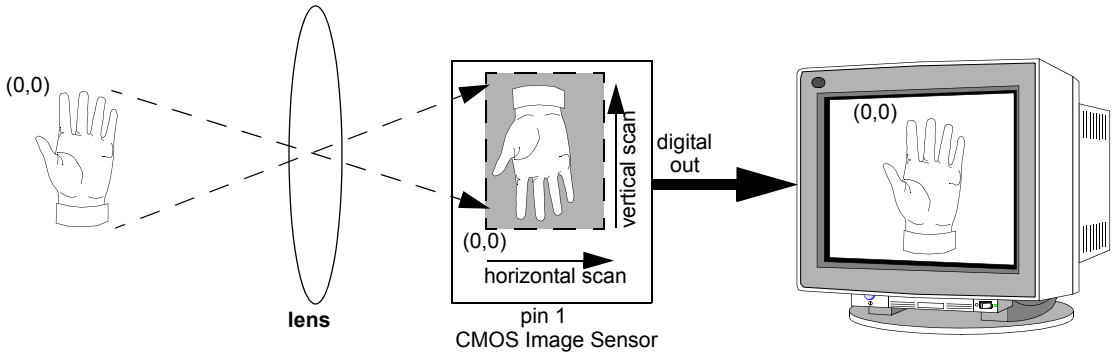


Figure 4. Scan directions and position of origin in imaging system

Pin Descriptions

Pin	Name	I/O	Typ	Description
1	d5	O	D	Digital output. Bit 5 of the digital video output bus. This output can be tri-stated
2	d6	O	D	Digital output. Bit 6 of the digital video output bus. This output can be tri-stated
3	d7	O	D	Digital output. Bit 7 of the digital video output bus. This output can be tri-stated
4	d8	O	D	Digital output. Bit 8 of the digital video output bus. This output can be tri-stated
5	d9	O	D	Digital output. Bit 9 of the digital video output bus. This output can be tri-stated
6	vdd_adc	I	P	3.0 volt supply for the 10 bit A/D converter.
7	vss_adc	I	P	0 volt supply for the 10 bit A/D converter.
8	vref_n	I	A	A/D reference resistor ladder low voltage. This is the bottom of the ADC reference ladder and is normally bypassed with a 10 μF capacitor.
9	vref_p	I	A	A/D reference resistor ladder high voltage. This is the top of the ADC reference ladder and is normally bypassed with a 10 μF capacitor.
10	vdd_ana	I	P	3.0 volt supply for analog circuits.
11	vss_ana	I	P	0 volt supply for analog circuits.
12	atest	O	A	Analog test pin. This pin is used for production testing and should not be connected.
13	resetb	I	D	Digital input with pull up resistor. When forced to a logic 0 the sensor is reset to its default power up state.
14	vdd_pix	I	P	3.0 volt supply for the pixel array. This pin should be connected to the 3.0v analog supply and bypassed to ground with a 10uF capacitor.
15	vss_od1	I	P	0 volt supply for the digital IO buffers
16	vdd_od1	I	P	3.0 volt supply for the digital IO buffers.
17	scanmode	I	D	Digital production test pin. This pin should be tied to ground
18	sda	IO	D	I^2C compatible serial interface data bus.
19	sclk	I	D	I^2C compatible serial interface clock.
20	vcp2	O	A	Analog output, reset charge pump 2 output, connect to vss_ana via a 0.1μf capacitor. Voltage on this pin should be 5 volt.
21	vcp1	O	A	Analog output, reset charge pump 1 output, connect to vss_ana via a 56pf capacitor. Voltage on this pin should be 3.6 volt.
22	hsync	IO	D	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, this pin is an output and is the horizontal synchronization pulse. When the sensor's digital video port is configured to be a slave, (the default), this pin is an input and is the row trigger.
23	vsync	IO	D	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, this pin is an output and is the vertical synchronization pulse. When the sensor's digital video port is configured to be a slave, (the default), this pin is an input and is the frame trigger.

Pin Descriptions (continued)

Pin	Name	I/O	Typ	Description
24	pclk	O	D	Digital output. The pixel clock.
25	mclk	I	D	Digital input. The sensor's master clock input.
26	vss_dig	I	P	0 volt power supply for the digital circuits.
27	vdd_dig	I	P	3.0 volt power supply for the digital circuits.
29	d1	O	D	Digital output. Bit 1 of the digital video output bus. This output can be tri-stated.
30	d2	O	D	Digital output. Bit 2 of the digital video output bus. This output can be tri-stated
31	d3	O	D	Digital output. Bit 3 of the digital video output bus. This output can be tri-stated
32	d4	O	D	Digital output. Bit 4 of the digital video output bus.This output can be tri-stated

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog).

Absolute Maximum Ratings (Notes 1 & 2)

Any Positive Supply Voltage	4.2V
Voltage On Any Input or Output Pin	-0.3V to 4.2V
Input Current at any pin (Note 3)	±35mA
Package Input Current (Note 3	±50mA
Package Dissipation at T_A = 25°C	see Note 4
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Machine Model	200V
Peak Soldering Temperature (Note 6)	235°C
Storage Temperature	-40°C to 125°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	-10°C≤T≤+50°C
All VDD Supply Voltages	+2.7V to +3.3V

DC and logic level specifications

The following specifications apply for all VDD pins= +3.0V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
sclk, sda Digital Input/Output Characteristics						
VIH	Logical “1” Input Voltage		0.7*vdd_od		vdd_od+0.5	V
VIL	Logical “0” Input Voltage		-0.5		0.3*vdd_od	V
VOL	Logical “0” Output Voltage	vdd_od = +2.7V, Iout=3.0mA			0.4	V
V_{hys}	Hysteresis *(SCLK pin only)*	vdd_od > +2.0V	0.05*vdd_od			V
I_{leak}	Input Leakage Current	Vin=vdd_od		1		µA
mclk, resetb, hsync, vsync Digital Input Characteristics						
VIH	Logical “1” Input Voltage	vdd_dig = +3.3V	2.0			V
VIL	Logical “0” Input Voltage	vdd_dig = +2.7V			0.8	V
IIH	Logical “1” Input Current	VIH = vdd_dig		1		nA
IIL	Logical “0” Input Current	VIL = vss_dig		-1		nA
d0 - d9, pclk, hsync, vsync Digital Output Characteristics						
VOH	Logical “1” Output Voltage	vdd_od=2.7V, Iout=-1.6mA	2.2			V
VOL	Logical “0” Output Voltage	vdd_od=2.7V, Iout =-1.6mA			0.5	V
IOZ	TRI-STATE Output Current	VOUT = vss_od VOUT = vdd_od		-0.1 0.1		µA µA
IOS	Output Short Circuit Current			+/-17		mA
Power Supply Characteristics						
IA	Analog Supply Current	Power down mode Operational mode	 @27MHz @12MHz	670 60 50		µA mA mA
ID	Digital Supply Current	Power down mode Operational mode	 @27MHz @12MHz	0 28 13		µA mA mA

Power Dissipation Specifications

The following specifications apply for all VDD pins= +3.0V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
P_{dwn}	Power Down			2.0		mW
PWR	Average Power Dissipation	@27 MHz @12MHz		264 189		mW mW

Video Amplifier Specifications

The following specifications apply for all VDD pins= +3.0V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
	Gain Resolution			7		Bits
	Step Size	(Gain / Resolution)		0.125		dB
	Maximum Gain			16		dB
	Minimum Gain			0.0		dB

AC Electrical Characteristics

The following specifications apply for All VDD pins = +3.0V. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
F_{mclk}	Input Clock Frequency		12		27	MHz
T_{ch}	Clock High Time	@ CLK_{max}	16.0			ns
T_{cl}	Clock Low Time	@ CLK_{max}	16.0			ns
	Clock Duty Cycle	@ CLK_{max}	45/55	50/50	55/45	min/max
T_{rc}, T_{fc}	Clock Input Rise and Fall Time			3		ns
F_{hclk}	Internal System Clock Frequency		12		27	MHz
T_{reset}	Reset pulse width		1.0			µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to **vss_dig** = **vss_ana** = **vss_adc** = **vss_od1** = **vss_od2** = 0V, unless otherwise specified.

Note 3: When the voltage at any pin exceeds the power supplies (VIN < [**vss_dig** or **vss_ana** or **vss_adc** or **vss_od1** or **vss_od2**] or VIN > [**vdd_dig** or **vdd_ana** or **vdd_adc** or **vdd_od1** or **vdd_od2**]), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA to two.

Note 4: The absolute maximum junction temperature (TJmax) for this device is 150°C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (Θ_{JA}), and the ambient temperature (TA), and can be calculated using the formula PDMAX = (TJmax - TA)/Θ_{JA}. In the 48-pin LCC, Θ_{JA} is 69°C/W, so PDMAX = 1,811mW at 25°C and 1,449 mW at the maximum operating ambient temperature of 50°C. Note that the power dissipation of this device under normal operation will typically be about 215 mW. The values for maximum power dissipation listed above will be reached only when the KAC-9647 is operated in a severe fault condition.

Note 5: Human body model is 100pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220pF discharged through ZERO Ohms.

Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The analog inputs are protected as shown below. Input voltage magnitude up to 500mV beyond the supply rails will not damage this device. However, input errors will be generated If the input goes above AV+ and below AGND.

Note 8: Typical figures are at TJ = 25°C, and represent most likely parametric norms

Note 9: Test limits are guaranteed to AOQL (Average Outgoing Quality Level).

CMOS Active Pixel Array Specifications

Parameter	Value	Units
Number of pixels (row, column) Total Active	 488 x 672 488 x 648	 pixels pixels
Array size (x,y Dimensions) Total Active	 2.93 x 4.03 2.93 x 3.89	 mm mm
Pixel Pitch	6.0	µ
Fill Factor without micro-lens	49	%

Image Sensor Specifications

The following specifications apply for All VDD pins = +3.3V, T_A = 25°C, Illumination Color Temperature = 2850°K, IR cutoff filter at 700nm, **mclk** = 27MHz, frame rate = 15Hz, unity video gain.

Parameter	Description	Min note 9	Typical note 8	Max note 9	Units
Optical Sensitivity[1] red green blue	Measured at the input of the A/D		 2.50 1.18 0.59		Volt/lux.s
Dark Signal	The pixel output signal due to dark current.		0.15		Volt/s
Read Noise	The RMS temporal noise of the pixel output signal in the dark averaged over all pixels in the array.		1.5		LSBs
Dynamic Range	The ratio of the saturation pixel output signal and the read noise expressed in dB.		57		dB
FPN	Fixed Pattern Noise: the RMS spatial noise in the dark excluding the effect of read noise.		0.2		%
PRNU red green blue	Photo Response Non Uniformity: the RMS variation of pixel sensitivities as a percentage of the average optical sensitivity.		 0.5 1.7 2.5		%

1 The optical sensitivity at the A/D output, in units of LSBs/lux.s, can be calculated using: $\frac{1024}{\text{vrefp-vrefn}} \cdot$ Optical Sensitivity

Sensor Response Curves

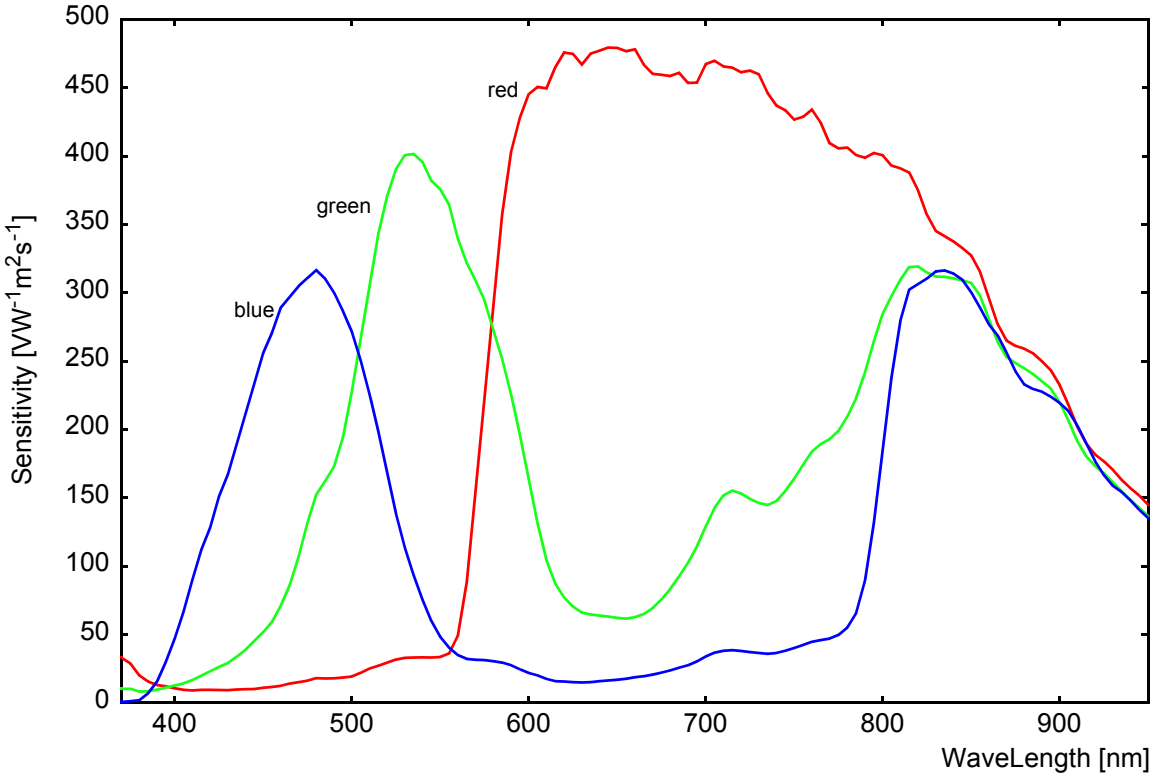


Figure 5. Spectral Response Curve

Functional Description

1.0 OVERVIEW

1.1 Light Capture and Conversion

The KAC-9647 contains a CMOS active pixel array consisting of 488 rows by 648 columns. 24 columns of optically shielded (black) pixels are provided to the right of the array as shown in Figure 6. Only the middle 8 black columns are used for black level compensation. The black pixels are physically located at the end of each row but are read out first.

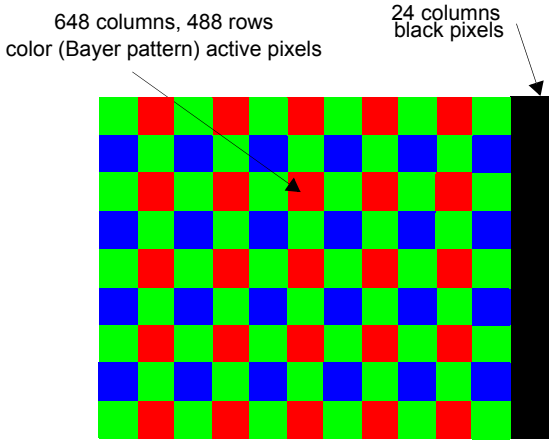


Figure 6. CMOS APS region of the KAC-9647

The color filters are Bayer pattern coded starting at row 0 and column 0. The color coding is green, red, green, red until the column 647 of row 0, then blue, green, blue, green until column 647 of row 1 and so on (see Figure).

At the beginning of a given integration time the on-board timing and control circuit will reset every pixel in the array one row at a time as shown in Figure 7. Note that all pixels in the same row are simultaneously reset, but not all pixels in the array.

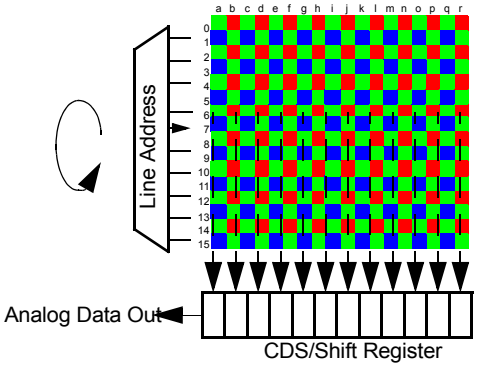


Figure 7. CMOS APS Row and Column addressing scheme

At the end of the integration time, the timing and control circuit will address each row and simultaneously transfer the integrated value of the pixel to a correlated double sampling circuit and then to a shift register as shown in Figure 7.

Once the correlated double sampled signals have been loaded into the shift register, the timing and control circuit will shift them out one pixel at a time.

The analog pixel signals are then separated and fed into four channels analog gain channels as shown in figure 8. Each gain channel can be digitally programmed allowing signal level of each color in the Bayer pattern to be seperately adjusted.

After color gain adjustment the analog value of each pixel is converted to a 10 bit digital data as shown in figure 8.

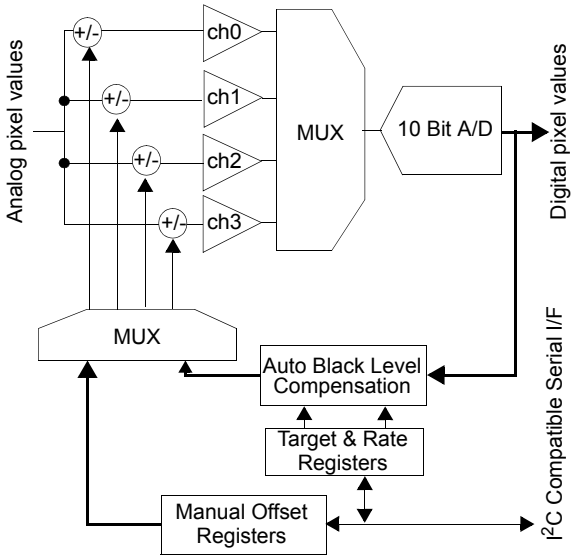


Figure 8. Analog Signal Conditioning & Conversion to Digital

The black level of each color together with the full analog signal path offset is automatically compensated as shown in figure 8. This can be manually overridden.

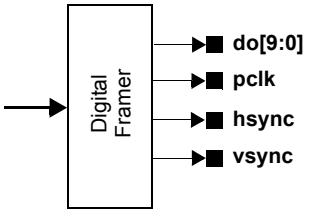


Figure 9. Digital Pixel Processing.

Finally the pixel data is framed and output on the digital video bus as shown in figure 9.

1.2 Program and Control Interfaces

The programming, control and status monitoring of the KAC-9647 is achieved through a two wire I^2C compatible serial bus. A device address pin is provided allowing two different device addresses to be selected for the serial interface as shown in Figure 10.

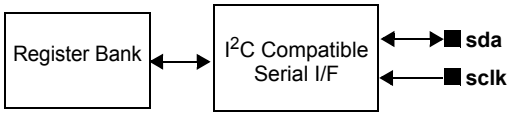


Figure 10. Control Interface to the KAC-9647.

Functional Description (continued)

2.0 DOUBLE BUFFERED REGISTERS

All programmable registers that effect the frame rate and integration timing are double buffered; such that the new values only take effect at the start of the new frame. When writing to all split double buffered registers, e.g. ITIMEH and ITIMEL, the following procedure must be followed:

- to change both the MSB and LSB, first write to the MSB register and then write to the LSB register,
- to change only the MSB, first write to the MSB register and then write the unchanged value of the LSB to the LSB register,
- to only change the LSB write to the LSB register.

3.0 WINDOWING

The integrated timing and control circuit allows any size window in any position within the active region of the array to be read out with a 4x4 pixel resolution. The window read out is called the "*Active Window*".

Four coordinates (start row address, start column address, end row address & end column address) need to be programmed to define the size and location of the "*Active Window*" to be read out (*see Figure 11*).

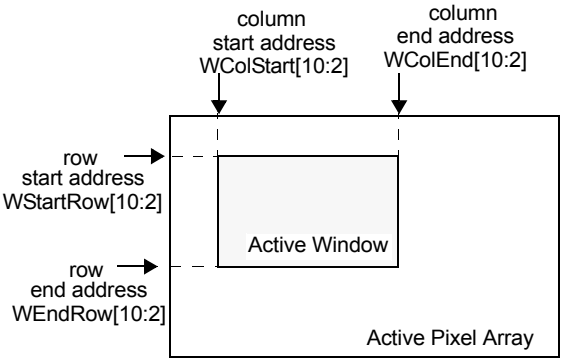


Figure 11. Windowing

Notes:

- By default the "*Active Window*" is set to 320 columns by 240 rows. To program a VGA window aligned to the optical center to the pixel array the following codes need to be written to the windowing registers via the I^2C interface

19h	WROWS	00h
1Ah	WROWE	3Bh
1Bh	WROWLSB	23h
1Ch	WCOLS	00h
1Dh	WCOLE	50h
1Eh	WCOLLSB	23h

- The "*Active Window*" registers are double buffered.
- The black pixels are read out at the beginning of each row even when not contained in the active window. The black pixel read out can be masked by setting the *BlKPixelEn* bit in the DVBUSCONFIG2 register to a logic 0.

4.0 ARRAY READOUT

The pixels in the array are read out in progressive scan. In progressive scan, every pixel in every row in the defined "*Active Window*" is consecutively read out, one pixel at a time. The first 8 pixels of every row are black unless masked out by setting the *BlkPixelEn* bit of the DVBUSCONFIG2 register to a logic 0.

The scan direction can be programmed as follows:

Scan Direction	VScanDir	HScanDir
Default Scan Direction	1	1
Reverse Vertical Scan Direction	0	1
Reverse Horizontal Scan Direction	1	0
Reverse Vertical and Horizontal Scan Direction	0	0

4.1 Default Scan Direction

The default scan direction is to consecutively read out, one pixel at a time, starting with the left most pixel in the top most row. Hence, for the example shown in Figure 12, the read out order will be *a0,b0,...,r0* then *a1,b1,...,r1* and so on until pixel *r20* is read out. See figure 12.

4.2 Reverse Vertical Scan Direction

The vertical scan direction can be reversed by setting the "VScanDir" bit in the VSCAN register to a logic 0, while setting the HScanDir bit in the HSCAN register to a logic 1. In this case for the example shown in Figure 12, the read out order will be *a10,b10,...,r10* then *a9,b9,...,r9* and so on until pixel *r0* is read out.

4.3 Reverse Horizontal Scan Direction

The horizontal scan direction can be reversed by setting the "HScanDir" bit in the HSCAN register to a logic 0, while setting the "VScanDir" bit in the VSCAN register to a logic 1. In this case for the example shown in Figure 12, the read out order will be *r0,q0,...,a0* then *r1,q1,...,a1* and so on until pixel *a10* is read out.

4.4 Reversing The Horizontal & Vertical Scan Direction

The horizontal scan direction can be reversed by setting both the "HScanDir" bit in the HSCAN and the "VScanDir" bit in the VSCAN register to a logic 0. In this case for the example shown in Figure 12, the read out order will be *r10,q10,...,a10* then *r9,q9,...,a9* and so on until pixel *a0* is read out.

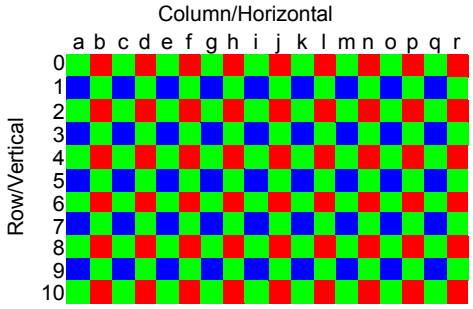


Figure 12. Progressive Scan Read Out Mode

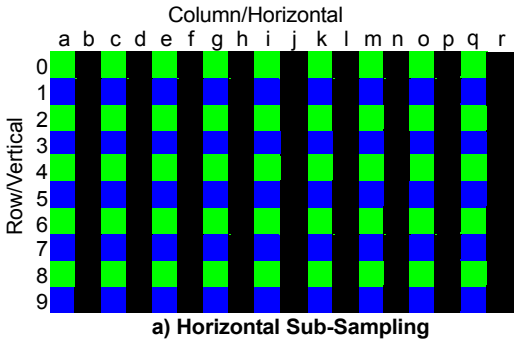
Functional Description (continued)

5.0 SUB-SAMPLING MODES

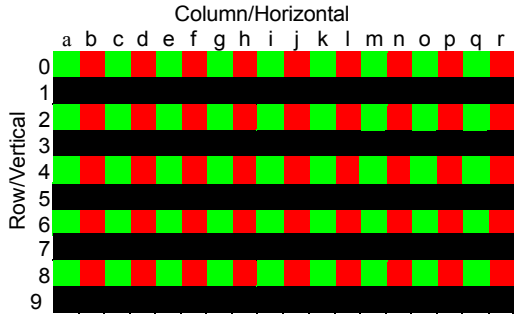
5.1 2:1 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the “Active Window” vertically, horizontally or both, with an aspect ratio of 2:1 as illustrated in figure 13.

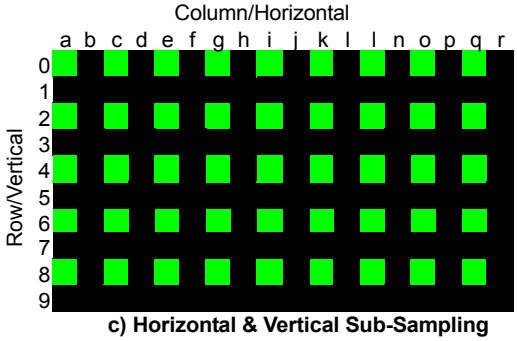
Register Bit	VIDCONFIG *Color*	VSCAN *VSub*	HSCAN *HSub*
Vertical	0	1	0
Horizontal	0	0	1
Both	0	1	1



a) Horizontal Sub-Sampling



b) Vertical Sub-Sampling



c) Horizontal & Vertical Sub-Sampling

Green Pixel Red Pixel Blue Pixel Not Read Out

Figure 13. Example of 2:1 Sub-sampling

Note a: Note that the pixel read out will depend on the programmed scan order as described in section 4.0.

Note b: For max FPN performance it is recommended to always switch on the averaging feature when sub-sampling (see next section).

5.2 2:1 Sub-Sampling with Averaging

The timing and control circuit can be programmed to average neighboring pixels in the analog domain before sub-sampling in the horizontal direction only as shown in the table below

Register Bit	VIDCONFIG *Color*	VSCAN *VAvr*	HSCAN *HAvr*
Horizontal	0	0	1

When **horizontal** 2:1 subsampling with averaging is selected, neighboring pixels in the horizontal direction are combined as shown in figure 14. The value of the combined pixel is given by

$$H_1 + H_2$$

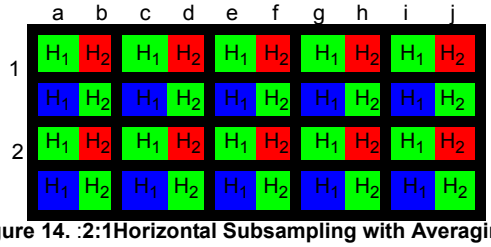


Figure 14. :2:1Horizontal Subsampling with Averaging

Functional Description (continued)

5.3 4:2 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the display window vertically, horizontally or both, with an aspect ratio of 4:2 as illustrated in figure 15

Register Bit	VIDCONFIG *Color*	VSCAN *VSub*	HSCAN *HSub*
Vertical	1	1	0
Horizontal	1	0	1
Both	1	1	1

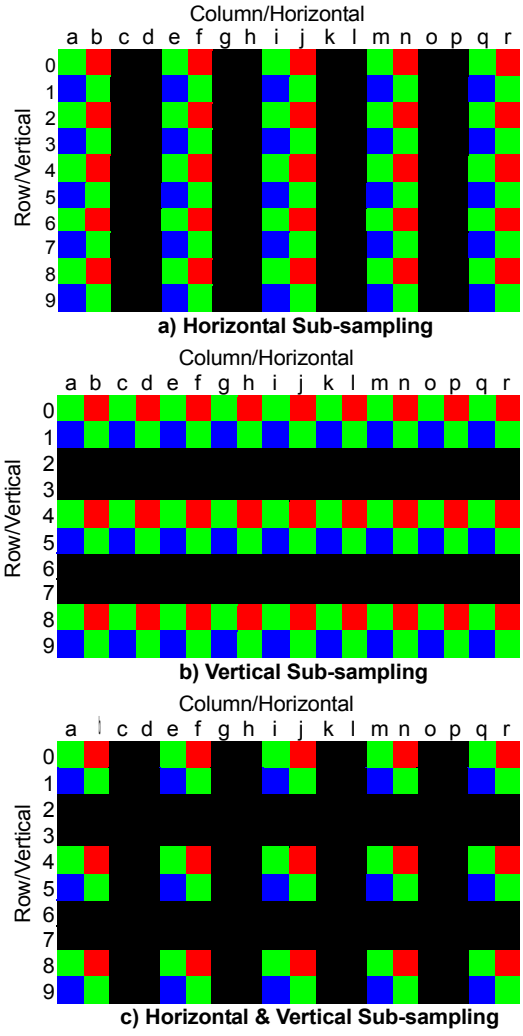


Figure 15. Example 4:2 Sub-sampling

Note a: Note that the pixel read out will depend on the programmed scan order as described in section 4.0.

Note b: For max FPN performance it is recommended to always switch on the averaging feature when sub-sampling (see next section).

5.4 4:2 Sub-Sampling with Averaging

The timing and control circuit can be programmed to average neighboring pixels of the same color in the analog domain before subsampling. This can be done in the horizontal direction only as shown in the table below:

Register Bit	VIDCONFIG *Color*	VSCAN *VAvr*	HSCAN *HAvr*
Horizontal	1	0	1

When **horizontal** 2:1 subsampling with averaging is selected, neighboring pixels in the horizontal direction are combined as shown in figure 16. The value of the combined pixel is given by

$$H_1 + H_2$$

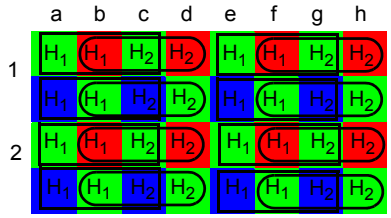


Figure 16. :4:2Horizontal Subsampling with Averaging

Functional Description (continued)

6.0 FRAME RATE & EXPOSURE CONTROL

6.1 Introduction

The frame time is defined as the time it takes to reset every pixel in the array, integrate the incident light, convert it to digital data and present it on the digital video port. This is not a concurrent process and is characterized in a series of events each requiring a certain amount of time as shown in Figure 17.

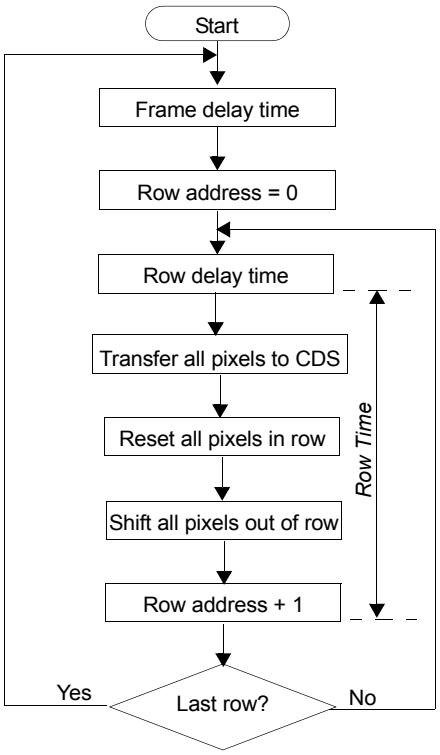


Figure 17. Frame Readout Flow Diagram

The following factors effect frame rate, exposure & signal level, the:

- frequency of *Hclk*
- size of the "*Active Window*"
- subsampling mode
- programmed row delay
- programmed frame delay.

The following factor effects signal level only.

- analog gain

The following factor effects exposure & signal level:

- integration time

This section describes how to program the frame rate and exposure time.

6.2 Analog Gain

Four channels of gain are provided allowing the gain of each color to be separately adjusted before the analog to digital conversion.

The mapping of each gain channel to a pixel in a quadrant is programmable, allowing flexibility in the selection of the Color Filter Array (CFA) pattern.

The color mapping is programmed using the CFAMAP register as shown in figure 18. For the example shown in figure 18 pixel "a1" can be routed to color gain channel 0 (ch0) by setting *ColorMap0* in the CFAMAP to 00. Pixel "a1" is to be routed to color gain channel 1 (ch1) by setting *ColorMap0* in the CFAMAP register should be set to 01.

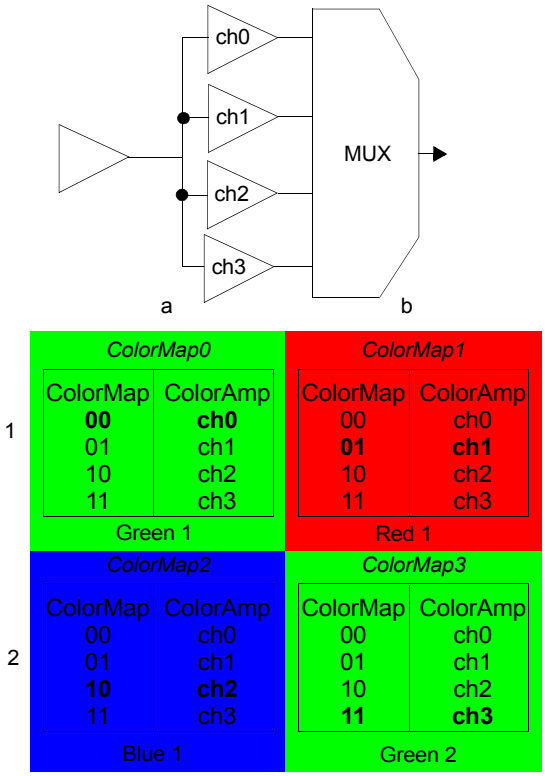


Figure 18. Color To Gain Channel Mapping

The KAC-9647 is supplied with a Bayer patterned CFA upon reset the color mapping is set as follows

Pixel Color	Gain Channel
Green 1	ch0
Red	ch1
Blue	ch2
Green 2	ch3

Each gain channel can provide up to 16dB of gain programmable in 128 steps of 0.125dB, (see registers PGA0, PGA1, PGA2 & PGA3).

Functional Description (continued)

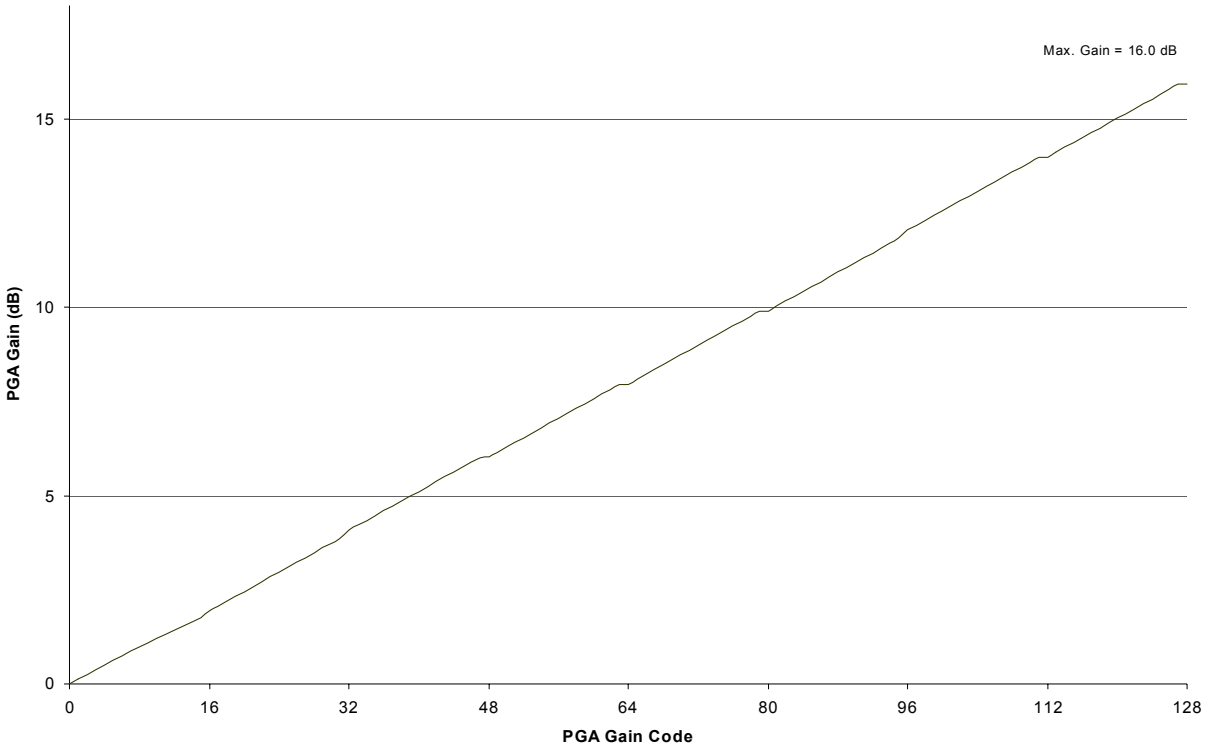


Figure 19. Gain Plot

6.3 Clock Generation

The KAC-9647 contains a clock generation module (figure 20) that will create three clocks as follows:

Hclk, the horizontal clock. This is an internal system clock and can be programmed to be the input clock *(***mclk***)* or **mclk** divided by 2,4 or 6. All exposure times are in multiples of this clock.

To set the frequency of this clock the *HclkGen* bits in the VCLKGEN register should be programed.

pclk the pixel clock. This is the external pixel clock that appears at the digital video port. By default **pclk** is free running and it's frequency is always equal to *Hclk* (see figure 20).

pclk can be programmed to the following modes:

- Data Ready Mode, where **pclk** clock will go active every time a valid pixel appears on the data out bus by setting the *PixClkMode* bit of the DVBUSCONFIG1 to a logic 1.
- Reverse Polarity Mode, where the polarity of **pclk** is negated by programming the *PixClk-Pol* bit in the DVBUSCONFIG2 register.

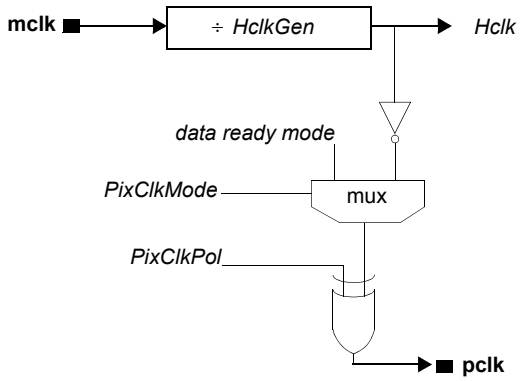


Figure 20. Clock Generation Module

Functional Description (continued)

6.4 Full Frame Integration

Full frame integration is when each pixel in the array integrates light incident on it for the duration of a frame (see Figure 21).

The number of pixels processed per row is given by:

$$N_{pix} = WEndCol - WStartCol + 1$$

Where:

WEndCol is the "Active Window" column start address as programmed in registers WCOLE and WCOLLSB.

WStartCol is the "Active Window" column end address as programmed in registers WCOLS and WCOLLSB.

The number of *Hclk* clock cycles required to process & shift out one row of pixels is given by:

$$RN_{Hclk} = R_{opcycle} + R_{Itime} + (N_{pix} * MH_{factor}) + R_{delay}$$

Where:

$R_{opcycle}$ is a fixed integer value of 137 representing the *Row Operation Cycle Time* in multiples of *Hclk* clock cycles. It is the time required to carry out all fixed row operations outlined in Figure 17.

R_{Itime} When partial frame integration is enabled, (*PrtFrmEn* bit in the ITIMECONFIG register is set to a logic 1), R_{Itime} is a fixed integer of 37. When Partial frame integration is disabled, (*PrtFrmEn* bit in the ITIMECONFIG register is set to a logic 0), R_{Itime} is a fixed integer of 0.

N_{pix} Is the number of pixels processed in a row.

MH_{factor} Is 1 when horizontal subsampling is disabled and 0.5 when horizontal subsampling is enabled.

R_{delay} a programmable value between 0 & 8191 representing the Row Delay Time in multiples of *Hclk*. This parameter allows the Row Operation Cycle time to be extended. The *Rdelay* value is programmed in the RDELAYH and RDELAYL registers.

The number of rows in the active window is given by:

$$N_{rows} = (WEndRow - WStartRow + 1) * MV_{factor}$$

Where:

WEndRow is the "Active Window" row start address as programmed in registers WROWE and WROWLSB.

WStartRow is the "Active Window" row end address as programmed in registers WROWS and WROWLSB.

MV_{factor} is 1 when vertical subsampling is disabled and 0.5 when vertical subsampling is enabled.

The number of *Hclk* clocks required to process a full frame is given by:

$$FN_{Hclk} = [N_{rows} + Fdelay] * RN_{Hclk}$$

Where:

N_{rows} is the number of rows in the "Active Window".

F_{delay} a programmable value between 0 & 32766 representing the *Inter Frame Delay* in multiples of RN_{Hclk}. This parameter allows the frame time to be extended. (See the Frame Delay High and Frame Delay Low registers). The *Fdelay* value is programmed in the FDELAYH and FDELAYL registers.

The frame rate is given by:

$$Frame\ Rate = \frac{Hclk}{FN_{Hclk}}$$

6.5 Partial Frame Integration

In some cases it is desirable to reduce the time during which the pixels in the array are allowed to integrate incident light without changing the frame rate.

This is known as *Partial Frame Integration* and can be achieved by resetting pixels in a given row ahead of the row being selected for readout as shown in Figure 21. The number of *Hclk* clocks required to process a partial frame is given by:

$$FP_{Hclk} = RN_{Hclk} * Itime$$

Where:

RN_{Hclk} is the number of *Hclk* clock cycles required to process & shift out one row of pixels.

Itime a programmable value between 0 & 32767 representing the number of rows ahead of the current row to be reset. This value must not be larger than the number of active rows. The *Itime* value is programmed in the ITIMEH and ITIMEL registers.

Note:

Upon system reset the partial frame integration is automatically enabled. It can be disabled by setting the *PrtFrmEn* bit in the ITIMECONFIG register to a logic 0 or by programming 0.

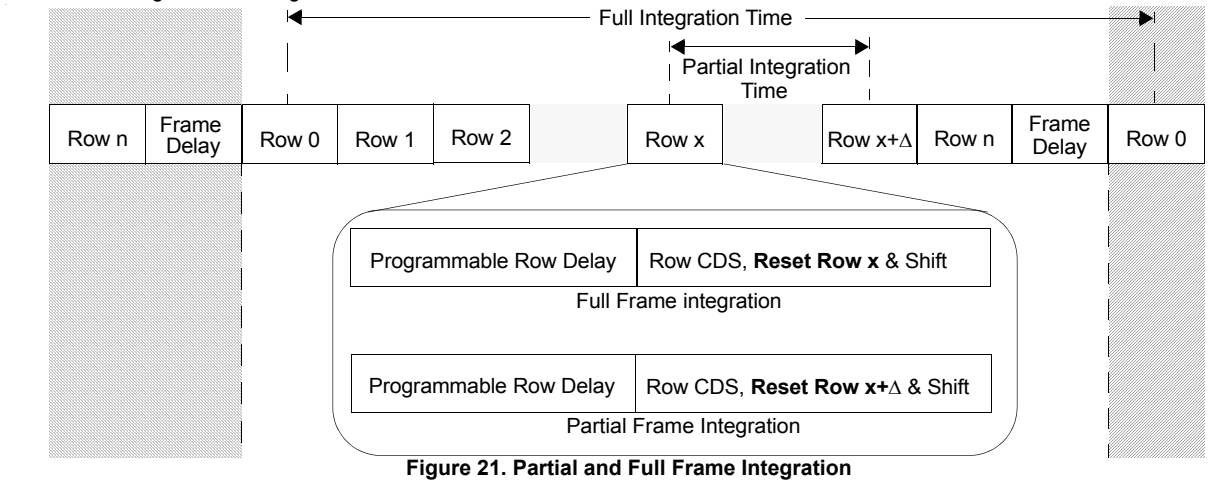


Figure 21. Partial and Full Frame Integration

Functional Description (continued)

7.0 BLACK LEVEL & OFFSET ADJUSTMENT

The KAC-9647 allows for both fine and coarse black level adjustment. Coarse adjustment is made using the PIXELOFFSET register and only needs to be done once at power up. Fine offset adjustment is done on a row basis and can be accomplished either atomically using the on chip black level compensation circuit or manually by disabling the on chip black level compensation circuit.

7.1 Coarse Black Level and Offset Adjustment

To ensure maximum performance of the CMOS image sensor, the natural offset of the pixel array needs to be minimized. Coarse adjustment is made using the PIXELOFFSET register and only needs to be done once at power up. This procedure is explained in detail in KAC-9647 Application Note 4.

7.2 Manual Black Level and Offset Adjustment

Each offset channel can provide up to 255 levels of black level and offset adjustment. To manually adjust the black level and offset the *BlkLevEn* bit in the BLKLEVCONFIG register should be set to a logic 1. Eight bit offset values can then be programmed to registers OFFSET0, OFFSET1, OFFSET2 & OFFSET3.

7.3 Auto Black Level and Offset Adjustment

Automatic black level and offset adjustment mode is enabled by setting the *BlkLevEn* bit in the BLKLEVCONFIG register to a logic 0.

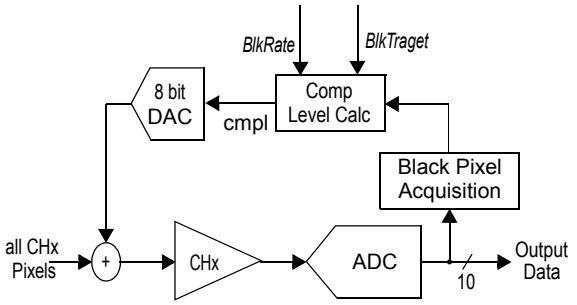


Figure 22: Digital Black Level & Offset Adjustment Loop

Figure 22 illustrates the automatic black level and offset compensation circuit contained within the sensor. For every row, the digitized values of the middle 8 black pixels are acquired and fed to the compensation level calculator circuit. This circuit is a digital first order exponential averaging filter. It calculates the compensation level (cmpl) that is required to ensure that for pixels that are optically black, the black level at the output of the ADC is equal to the desired black level. The desired black level (ClkTarget) can be programmed in the BLKTARGET register.

The black level control loop not only controls the black level of the pixels in the sensor array, but also controls the offset of the PGAs and A/D in the system. Because there are four channels, which can be operating at different gains and with different offsets, four different compensation levels are calculated, one for each channel.

The convergence rate of the cancellation loop can be set by programming the *BlkRate* parameter located in the BLKLEVCONFIG register. Small values of the *BlkRate* parameter ensure a fast convergence. High values of the *BlkRate* parameter reduce the noise in the calculated compensation level. The optimal setting of the *BlkRate* parameter is the result of a compromise between convergence speed after power up and image quality.

8.0 SYSTEM MANAGMENT

8.1 System Reset

Upon power up an on-chip power on reset block will ensure that the sensor is initialized to its reset state. After power up the sensor can be reset by asserting a logic 0 on the **resetb** pin or by writing to the *SenReset* bin in the PWD&RESET register.

Furthermore, all state machines contained in the sensors integrated timing and control block can be reset by writing to the *RstzSoft* bit in the OPCTRL register.

8.2 Power Up and Down

The KAC-9647 is equipped with an on-board power management system allowing the analog and digital circuitry to be switched off (power down) and on (power up) at any time.

The sensor can be put into power down mode by asserting a logic one on the **pdwn** pin or by writing to the *PwDn* bit in the PWD&RST register.

To power up the sensor a logic zero can be asserted on the **pdwn** pin or by writing to the *PwDn* bit in the PWD&RST register.

To ensure proper sensor operation the reference ladders must be intitialized upon power up of the sensor.

To switch on the sensor's reference resistors, the following sequence of codes should be written to the sensor via the I^2C compatible interface at power up.

This must be done for the sensor to operate properly after reset or when the sensor is powered up.

Address (Hex)	Data (Hex)
INITREG2	01
POWCTRL	81

Functional Description

9.0 SERIAL BUS

The serial bus interface consists of the **sda** (serial data) and **sclk** (serial clock) pins. The KAC-9647 can operate only as a slave.

The **sclk** pin is an input, it only controls the serial interface, all other clock functions within KAC-9647 use the master clock pin, **mclk**. **Mclk** must be running at least 4 times faster than **sclk** to write to the serial bus.

9.1 Start/Stop Conditions

The serial bus will recognize a logic 1 to logic 0 transition on the **sda** pin while the **sclk** pin is at logic 1 as the ***start*** condition. A logic 0 to logic 1 transition on the **sda** pin while the **sclk** pin is at logic 1 is interrupted as the ***stop*** condition as shown in Figure 23.

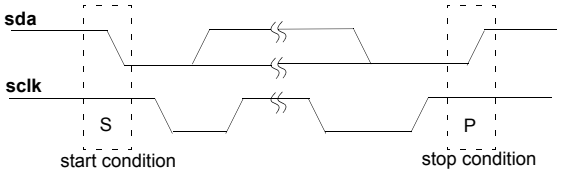


Figure 23. Start/Stop Conditions

9.2 Device Address

The *Device Address* can be changed by writing to the *I2cDevAddr* parameter in the I2CMODE Register.

9.3 Acknowledgment

The KAC-9647 will hold the value of the **sda** pin to a logic 0 during the logic 1 state of the *Acknowledge* clock pulse on **sclk** as shown in Figure 24.

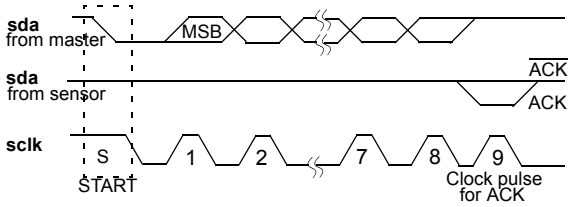


Figure 24. Acknowledge

9.4 Data Valid

The master must ensure that data is stable during the logic 1 state of the **sclk** pin. All transitions on the **sda** pin can onlyoccur when the logic level on the sclk pin is “0” as shown in Figure 25

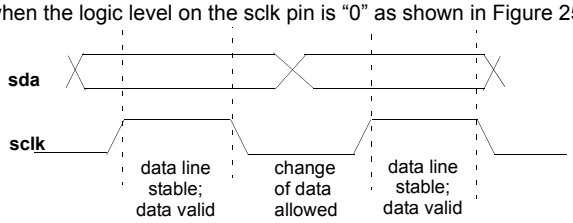


Figure 25. Data Validity

9.5 Byte Format

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an *Acknowledge*. The most significant bit of the byte is should always be transmitted first. See Figure 26.

9.6 Write Operation

A write operation is initiated by the master with a *Start Condition* followed by the sensor’s *Device Address* and $\overline{Write}$ bit. When the master receives an *Acknowledge* from the sensor it can transmit an 8-bit internal register address. The sensor will respond with a second *Acknowledge* signaling the master to transmit 8 write data bits. A third *Acknowledge* is issued by the sensor when the data has been successfully received.
The write operation is completed when the master asserts a *Stop Condition* or a second *Start Condition*. See Figure 27.

9.7 Read Operation

A read operation is initiated by the master with a *Start Condition* followed by the sensor’s *Device Address* and $\overline{Write}$ bit. When the master receives an *Acknowledge* from the sensor it can transmit the internal *Register Address* byte. The sensor will respond with a second *Acknowledge*. The master must then issue a new *Start Condition* followed by the sensor’s *Device Address* and *read* bit. The sensor will respond with an Acknowledged followed by the *Read Data* byte.
The read operation is completed when the master asserts a *Not Acknowledge* followed by *Stop Condition* or a second *Start Condition*. See Figure 28.

9.8 Advanced Write Mode

Several addresses can be written to without the need to re-start by setting the *AdvWr* bit in the I2CMODE register to a logic 1.

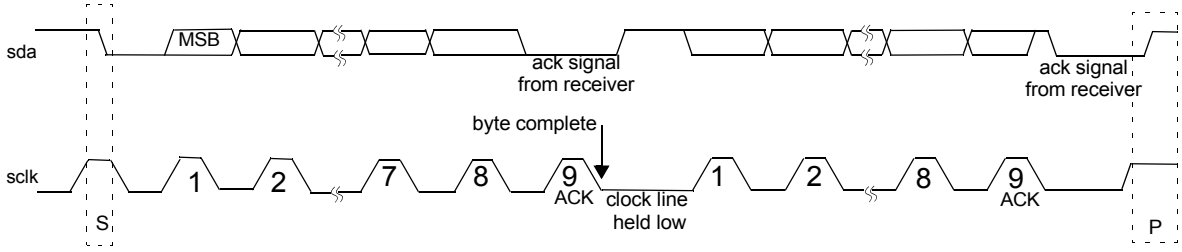


Figure 26. Serial Bus Byte Format

bold **sensor action**

Figure 27. Serial Bus Write Operation

bold **sensor action**

Figure 28. Serial Bus Read Operation

Functional Description (continued)

10.0 DIGITAL VIDEO PORT

The captured image is placed onto a flexible 10-bit digital port as shown in Figure 9. The digital video port consists of a programmable 10-bit digital Data Out Bus (**d[9:0]**) and three programmable synchronisation signals (**hsync**, **vsync**, **pclk**).

By default the synchronisation signals are configured to operate in "*slave*" mode. They can be programmed to operate in "*master*" mode.

The following sections are a detailed description of the timing and programming modes of digital video port.

The 10-bit digital video out bus can be tri-stated by asserting a logic 0 on the **oe** pin or by writing a logic 1 to the *TriState* bit in the DVBUSCONFIG3 register. In addition to this, the 10-bit digital video bus can be switch off to a logic 0 by writing a logic 0 to the *VBusEn* bit of the DVBUSCONFIG2 register (see figure 29).

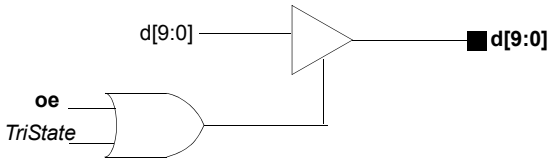


Figure 29. Digital Pixel Data Out Bus Circuit Diagram

10.1 Digital Video Data Out Bus (d[9:0])

A programmable barrel shifter is provided to map the output of the internal pixel data framer to the pins of the digital video bus as illustrated in Figure 30.

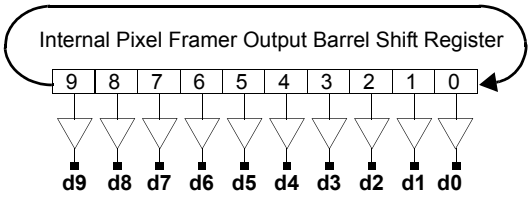


Figure 30. Digital Video Bus Switching Modes

The *Bshift* parameter in the DVBUSCONFIG2 register can be used to program the number of bits that the digital pixel data is shifted by.

This feature allows a programmable digital gain to be implemented when connecting the sensor to 8 or 10 bit digital video processing systems as illustrated in Figure 31.

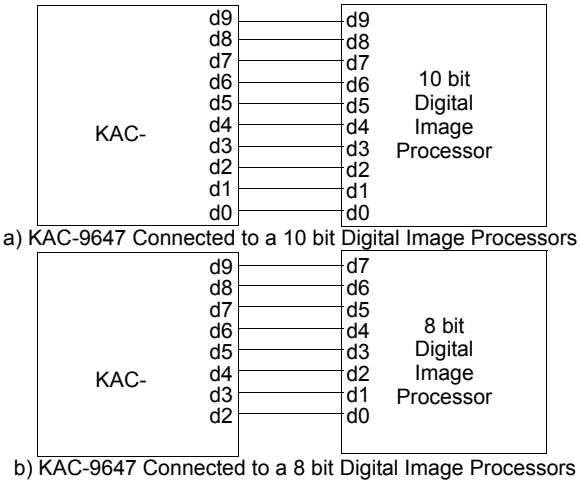


Figure 31. Example of connection to 10/8 bit systems

Synchronisation Signals in Master Mode

In master mode the integrated timing and control block controls the flow of data onto the 12-bit digital port, three synchronisation outputs are provided:

pclk is the pixel clock output pin.
hsync is the horizontal synchronisation output signal.
vsync is the vertical synchronisation output signal.

The **vsync**, **hsync** and **pclk** signals can be tri-stated by asserting a logic 0 on the **oe** pin or by writing a logic 0 to the *TriState* bit in the DVBUSCONFIG3 register. In addition to this **vsync**, **hsync** and **pclk** signals can be switch off by writing a logic 0 to the *VBusEn* bit of the DVBUSCONFIG2 register. (see figure 32)

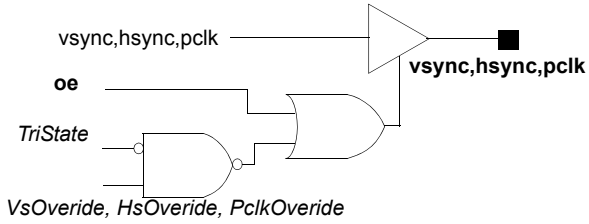


Figure 32. hsync,vsync and pclk output circuit diagram

10.2 Pixel Clock Output Pin (pclk) (Master Mode)

The pixel clock output pin, **pclk**, is provided to act as a synchronisation reference for the pixel data appearing at the digital video out bus pins **d[9:0]**. This pin can be programmed to operate in two modes:

- In free running mode, (the *PixClkMode* bit of DVBUSCONFIG1 register is set to a logic 0), the pixel clock output pin, **pclk**, is always running with a fixed period. Pixel data appearing on the digital video bus **d[9:0]** are synchronized to a specified active edge of the clock as shown in Figure 33.

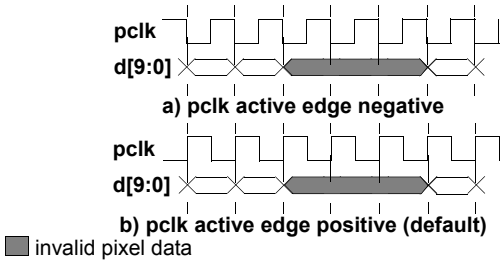


Figure 33. pclk in Free Running Mode

- In data ready mode, (the PixClkMode bit of DVBUSCONFIG1 register is set to a logic 1), the pixel clock output pin **pclk** will produce a pulse with a specified level every time valid pixel data appears on the digital video bus **d[9:0]** as shown in Figure 34.

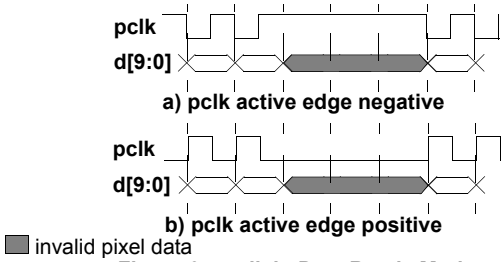


Figure 34. pclk in Data Ready Mode

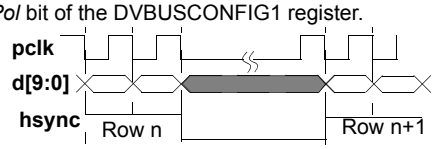
Functional Description (continued)

By default the pixel clock is a free running active high (pixel data changes on the positive edge of the clock) with a period equal to the internal *hclk*. See section 6.3 for more **pclk** programming modes.

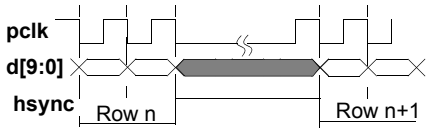
10.3 Horizontal Synchronisation Output Pin (hsync)

The horizontal synchronisation output pin, **hsync**, is used as an indicator for row data. The **hsync** output pin can be programmed to operate in two modes as follows:

- Level mode should be used when the pixel clock, **pclk**, is programmed to operate in *free running mode*. In level mode the **hsync** output pin will go to the specified level (high or low) at the start of each row and remain at that level until the last pixel of that row is read out on **d[9:0]** as shown in Figure 35. The **hsync** level is always synchronized to the active edge of **pclk**. The **hsync** pin is put into level mode by setting the *HsyncMode* bit of the DVBUSCONFIG1 register to a logic 0. The active level of the **hsync** pulse is programmed using the *HsyncPol* bit of the DVBUSCONFIG1 register.



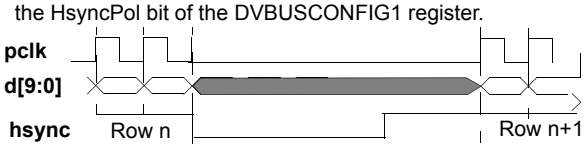
a) hsync programmed to be active high (default)



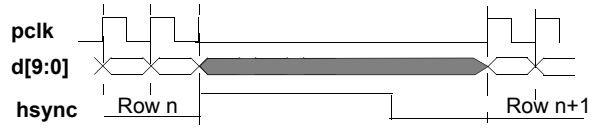
b) hsync programmed to be active low

Figure 35. hsync in Level Mode

- Pulse mode should be used when the pixel clock, **pclk**, is programmed to operate in *data ready mode*. In pulse mode the **hsync** output pin will produce a pulse at the end of each row. The width of the pulse will be a minimum of four **pclk** cycles and its polarity can be programmed as shown in Figure 36. The **hsync** level is always synchronized to the active edge of **pclk**. The **hsync** pin is put into pulse mode by setting the *HsyncMode* bit of the DVBUSCONFIG1 register to a logic 1.The active level of the **hsync** pulse is programmed using the HsyncPol bit of the DVBUSCONFIG1 register.



a) hsync programmed to be active high



b) hsync programmed to be active low

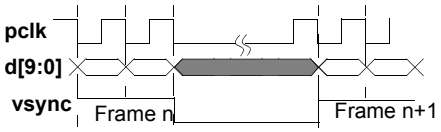
Figure 36. hsync in Pulse Mode

By default the first pixel data at the beginning of each row is placed on the digital video bus as soon as **hsync** is activated. Furthermore, **hsync** is de-activated upon the placement of the last pixel of the current row on the digital video bus the digital video bus. It is possible to shift the start and end edges of the **hsync** signal by programming the *HsyncStart* parameter of the DVBUSCONFIG0 register and the *HsyncEnd* parameter of the HYSNCADJUST register.

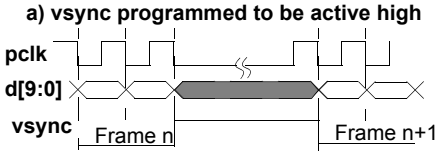
10.4 Vertical/Horizontal Synchronisation Pin (vsync)

The vertical synchronisation output pin, **vsync**, is used as an indicator for pixel data within a frame. The **vsync** output pin can be programmed to operate in two modes as follows:

- Level mode should be used when the pixel clock, **pclk**, is programmed to operate in *free running mode*. In level mode the **vsync** output pin will go to the specified level (high or low) at the start of each frame and remain at that level until the last pixel of that row in the frame is placed on **d[9:0]** as shown in Figure 37. The **hsync** level is always synchronized to the active edge of **pclk.** The **vsync** pin is put into level mode by setting the *VsyncMode* bit of the DVBUSCONFIG1 register to a logic 0. The active level of the **vsync** pulse is programmed using the *VsyncPol* bit of the DVBUSCONFIG1 register.



a) vsync programmed to be active high

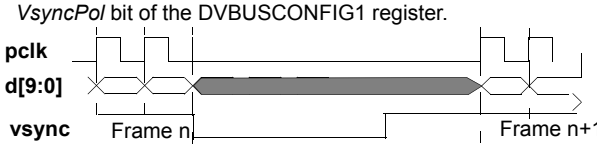


b) vsync programmed to be active low

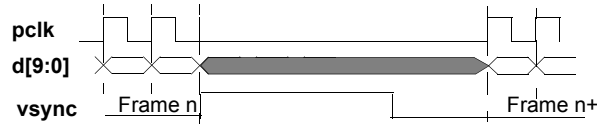
invalid pixel data

Figure 37. vsync in Level Mode

- Pulse mode should be used when the pixel clock, **pclk**, is programmed to operate in *data ready mode*. In pulse mode the **vsync** output pin will produce a pulse at the end of each frame. The width of the pulse will be a minimum of four **hclk** cycles and its polarity can be programmed as shown in Figure 38. The **vsync** level is always synchronized to the active edge of **pclk**. The **hsync** pin is put into pulse mode by setting the *HsyncMode* bit of the DVBUSCONFIG1 register to a logic 1. The active level of the **vsync** pulse is programmed using the *VsyncPol* bit of the DVBUSCONFIG1 register.



a) vsync programmed to be active high



b) vsync programmed to be active low (default)

invalid pixel data

Figure 38. vsync in pulse mode

By default the first pixel data at the beginning of each frame is placed on the digital video bus as soon as **vsync** is activated. Furthermore, **vsync** is de-activated upon the placement of the last pixel of the current frame on the digital video bus. It is possible to shift the start and end edges of the **vsync** signal by programming the *VsyncStart* parameter of the DVBUSCONFIG0 register and the *VsyncEnd* parameter of the HYSNCADJUST register.

Functional Description (continued)

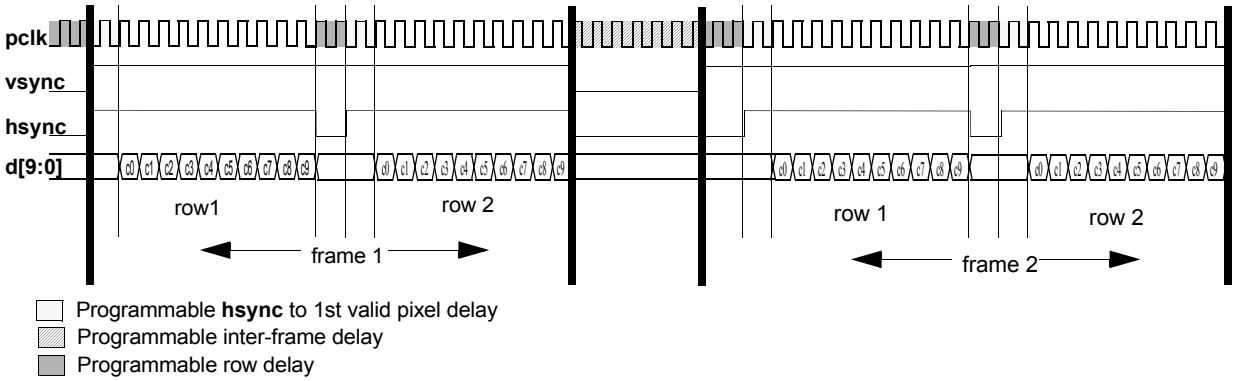


Figure 39. Example of Digital Video Port Timing in Progressive Scan Mode

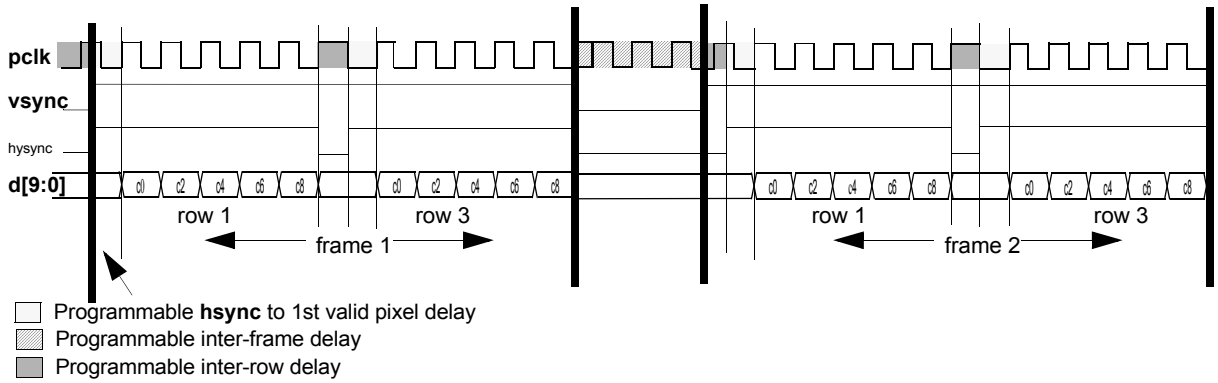


Figure 40. Example of Digital Video Port Timing in 2:1 Sub-sampling Mode

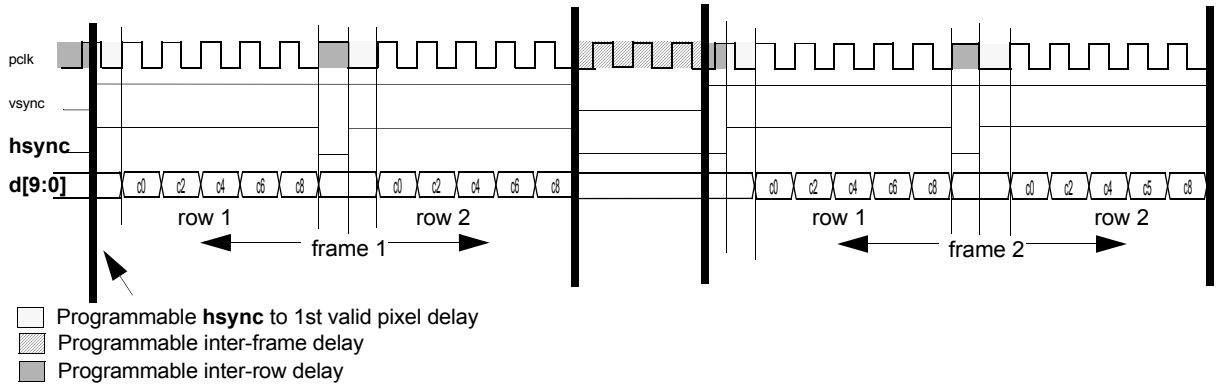


Figure 41. Example of Digital Video Port Timing in 4:2 Sub-sampling Mode

Functional Description (continued)

10.5 Synchronisation Signals in Slave Mode

By default the sensor's digital video port synchronisation signals are configured to operate in slave mode. In slave mode the integrated timing and control block will only start frame and row processing upon the receipt of triggers from an external source.

Note:

1. Partial frame integration is disabled in slave mode.
2. In order to get all rows out of the device in slave mode VsynPol and HsynPol bits of register 0x53h must be set to 0.

Only two synchronization signals are used in slave mode as follows:

hsync is the row trigger input signal.
vsync is the frame trigger input signal.

Figure 42 shows the KAC-9647's digital video port in slave mode connected to a digital video processor master DVP.

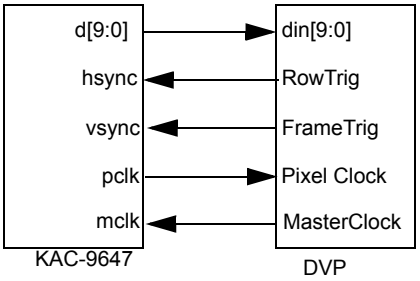


Figure 42. KAC-9647 in slave mode

10.6 Row Trigger Input Pin (hsync)

The row trigger input pin, **hsync**, is used to trigger the processing of a given row. It must be activated for at least two **mclk** cycles. The first pixel data will appear at **d[9:0]** "X_{mclk}"periods after the falling edge of the row trigger, where X_{mclk} is given by:

$$X_{mclk} = 146 + PrtFrmEn*37 - 8*BlkPixelEn$$

Where:

PrtFrmEn is the partial frame integration bit setting in the ITIMECONFIG register.
BlkPixelEn is the BlkPixelEn bit setting in the DVBUSCONFIG2 register

The polarity of the active level of the row trigger can be programmed using the HsynPol bit of the DVBUSCONFIG1 register. By default it is active high.

10.7 Frame Trigger Input Pin (vsync)

The frame trigger input pin, **vsync**, is used to reset the row address counter and prepare the array for row processing. It must be activated for at least one more **mclk** cycle than the row trigger and the falling edge must be between 1 and 96 **mclk** cycles after falling edge of **hsync** as illustrated in Figure 44.

The polarity of the active level of the frame trigger is programmable. By default it is active high.

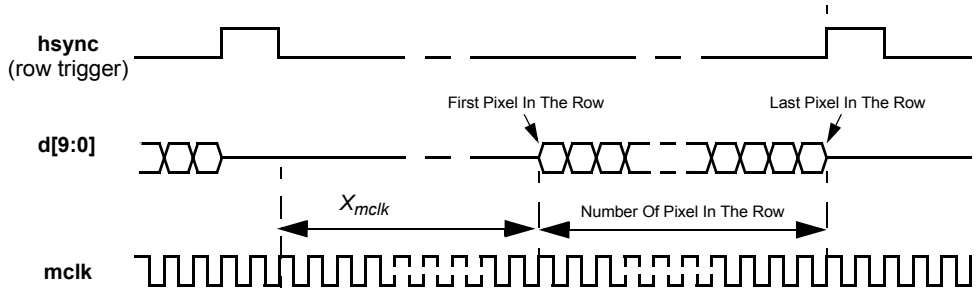


Figure 43. hsync slave mode timing diagram for centered display window of 640 pixels

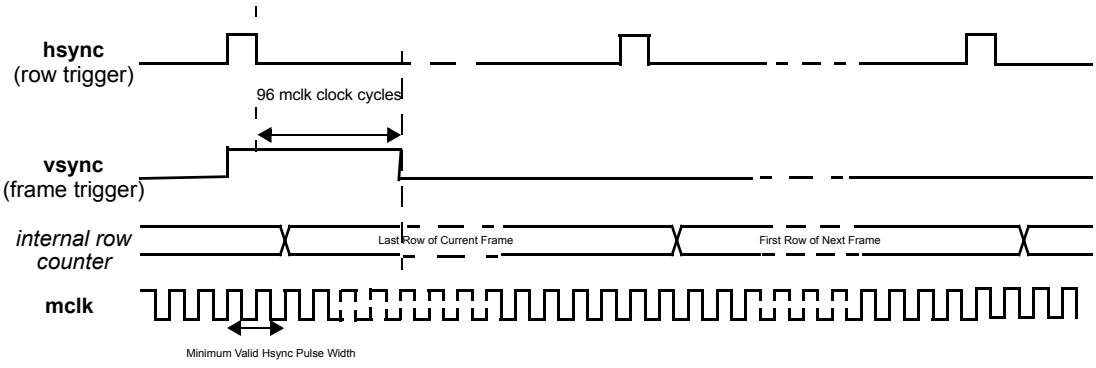


Figure 44. vsync slave mode timing diagram.

MEMORY MAP

ADDR	Register	Reset Value	Description
00h	DEVID	47h	Device ID Register.
01h	REV	Latest Silicon	Revision Register
02h - 04h			Reserved
05h	VCLKGEN	00h	Clock Generation Register
06h	PWD&RST	00h	Power Down & Reset Register
07h	I2CMODE	AAh	I^2C compatible Serial Interface Configuration Register
08h			Reserved
09h	OPCTRL	02h	Operation Control Register
0Ah - 0Fh		00h	Reserved
10h	VIDCONFIG	01h	Video Color Configuration Register
11h	VSCAN	04h	Vertical Scan Configuration Register
12			Reserved
1 3h	HSCAN	04h	Horizontal Scan Configuration Register
14h			Reserved
15h	ITIMECONFIG	08h	Integration Time Configuration Register
16h-18h			Reserved
19h	WROWS	00h	Active Window Row Start Register
1Ah	WROWE	16h	Active Window Row End Register
1Bh	WROWLSB	23h	Active Window Row LSB Register
1Ch	WCOLS	00h	Active Window Column End Register
1Dh	WCOLE	28h	Active Window Column Start Register
1Eh	WCOLE	23h	Active Window Column LSB Register
20h	FDELAYH	00h	Frame Delay High Register
21h	FDELAYL	08h	Frame Delay Low Register
22h	RDELAYH	00h	Row Delay High Register
23h	RDELAYL	08h	Row Delay Low Register
24h	ITIMEH	00h	Integration Time High Register
25h	ITIMEL	00h	Integration Time Low Register
26h - 3Fh			Reserved
40h	BLKLEV	07h	Black Level Compensation Register
41h	BLKTARGET	10h	Black Level Target Register
42h	PGA0	00h	Programmable Gain Amplifier, Channel 0
43h	PGA1	00h	Programmable Gain Amplifier, Channel 1
44h	PGA2	00h	Programmable Gain Amplifier, Channel 2
45h	PGA3	00h	Programmable Gain Amplifier, Channel 3
46h	OFFSET0	00h	Gain Channel 0 Offset Register
47h	OFFSET1	00h	Gain Channel 1 Offset Register
48h	OFFSET2	00h	Gain Channel 2 Offset Register
49h	OFFSET3	00h	Gain Channel 3 Offset Register
4Ah	CFAMAP	1Bh	Gain Color Map Register.
4Bh- 4Fh			Reserved

MEMORY MAP (continued)

ADDR	Register	Reset Value	Description
50h	VSYNCADUST	08h	Vsync Adjust Register
51h	HSYNCADUST	08h	Hsync Adjust Register
52h	DVBUSCONFIG0	00h	Digital Video Bus Configuration Register 0
53h	DVBUSCONFIG1	0Ch	Digtal Video Bus Configuration Register 1
54h	DVBUSCONFIG2	F0h	Digtal Video Bus Configuration Register 2
55h	DVBUSCONFIG3	00h	Digtal Video Bus Configuration Register 3
56h - 7Fh			Reserved
80h	INITREG1	00h	Sensor Initialization Register 1
81h - 82h			Reserved
83h	PIXELOFFSET	1Eh	Sensor's Pixel Offset Register
84h			Reserved
85h	POWCTRL	81h	Sensor's Power Down Control Register
86h - 87h			Reserved
88h	INITREG2	00h	Sensor Initialization Register 2

Register Set

The following section describes all available registers in the KAC-9647 register bank and their function.

Register Name **Device ID**
Address **00 Hex**
Mnemonic **DEVID**
Type **Read Only**
Reset Value **47 Hex**

Bit	Bit Symbol	Description
7:0	DevId	The sensor's device ID.

Register Name **Silicon Revision**
Address **01 Hex**
Mnemonic **REV**
Type **Read Only**
Reset Value **Latest Silicon Hex**

Bit	Bit Symbol	Description
7:0	SiRev	The sensor's silicon revision.

Register Name **Clock Generation Register**
Address **05 Hex**
Mnemonic **VCLKGEN**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7		Reserved.
2:1	HclkGen	Use to divide the frequency of the sensors master clock input, **mclk**, and generate the sensor's internal clock, *hclk.* 00 ÷1(default) 01 ÷2 10 ÷4 11 ÷6
0		Reserved.

Register Name **Power Down/Reset Register**
Address **06 Hex**
Mnemonic **PWD&RST**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:2		Reserved.
1	SenReset	Set this self clearing bit to a logic 1 to reset the sensor.
0	PwDn	Set to a logic 1 to power down the chip. All internal clocks will be turned off in this mode. Set to a logic 0, (the default) to put the chip in power up mode. Refer to section 8.2 for information on the low power down sequence.

Register Name **I^2C Mode Register**
Address **07 Hex**
Mnemonic **I2CMODE**
Type **Read/Write**
Reset Value **AA Hex.**

Bit	Bit Symbol	Description
7:1	I2cDevAddr	Use to program the I^2C compatible device address. By default, the value is 55 hex.
0	AdvWr	Set to a logic 1 to activate the I^2C compatible serial interface's advance write option. In advance write mode, several addresses can be written to without the need to restart. Set to a logic 0, the default, to operate the I^2C compatible interface in standard write mode.

Register Name **Operation Control Register**
Address **09 Hex**
Mnemonic **OPCTRL**
Type **Read/Write**
Reset Value **02 Hex.**

Bit	Bit Symbol	Description
7:3		Reserved.
2	MasterMode	Set to a logic 1 to configure the digital video port's synchronisation's signal to operate in master mode. Set to a logic 0 (the default) to configure the digital video port's synchronisation signals to operate in slave mode.
1		This bit is reserved for factory testing and must be set to a logic 1 at all times.
0	RstzSoft	Set this self clearing register to a logic 1 to reset all state machines contained in the integrated smart timing and control circuitry.

Register Set (continued)

Register Name Video Configuration Register
Address 10 Hex
Mnemonic VIDCONFIG
Type Read/Write
Reset Value 01 Hex.

Bit	Bit Symbol	Description
7:1		Reserved.
0	Color	Set to a logic 1, (the default), to configure the sensor's smart timing and control circuit to operate in color mode. This bit always be set for color sensor. Set to a logic 0 to configure the sensor's smart timing and control circuit to operate in monochrome mode.

Register Name Vertical Scan Register
Address 11 Hex
Mnemonic VSCAN
Type Read/Write (Double Buffered)
Reset Value 04 Hex.

Bit	Bit Symbol	Description
7:3		Reserved.
2	VscanDir	Set to a logic 1, (the default), to set the sensor's vertical scan direction to operate from top to bottom. Set to a logic 0, to set the sensor's vertical scan direction to operate from bottom to top.
1	VSub	Set to a logic 1 to enable vertical sub sampling. Set to a logic 0, (the default), to disable vertical sub sampling.
0		Reserved.

Register Name Horizontal Scan Register
Address 13 Hex
Mnemonic HSCAN
Type Read/Write (Double Buffered)
Reset Value 04 Hex.

Bit	Bit Symbol	Description
7:3		Reserved.
2	HscanDir	Set to a logic 1, (the default) to set the sensor's horizontal scan direction to operate from left to right. Set to a logic 0, to set the sensor's horizontal scan direction to operate from right to left.
1	HSub	Set to a logic 1 to enable horizontal sub sampling. Set to a logic 0, (the default), to disable horizontal sub sampling.
0	HAvrg	Set to a logic 1 to enable horizontal averaging. Set to a logic 0, (the default) to disable horizontal averaging.

Register Name Integration Time Configuration Register
Address 15 Hex
Mnemonic ITIMECONFIG
Type Read/Write (Double Buffered)
Reset Value 08 Hex.

Bit	Bit Symbol	Description
7:4		Reserved.
3	PrtFrmEn	Set to a logic 1, (the default), to turn on the Partial Frame Integration. Set to a logic 0, to turn off the partial Partial Frame Integration.
2:0		Reserved, should always be set to a logic 0.

Register Set (continued)

Register Name Active Window Row Start Register
Address 19 Hex
Mnemonic WROWS
Type Read/Write (Double Buffered)
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	WStar-tRow[10:3]	Use to program the display window's start row address' MSBs. The LSBs can be programmed using the DROWLSB register.

Register Name Active Window Row End Register
Address 1A Hex
Mnemonic WROWE
Type Read/Write (Double Buffered)
Reset Value 1B Hex.

Bit	Bit Symbol	Description
7:0	WEnd-Row[10:3]	Use to program the scan window's end row address' MSBs. The LSBs can be programmed using the WROWLSB register.

Register Name Active Window Row LSB Register
Address 1B Hex
Mnemonic WROWLSB
Type Read/Write (Double Buffered)
Reset Value 23 Hex.

Bit	Bit Symbol	Description
7:6		Reserved
5	WStartRow[2]	Use to program the display window's start row address LSBs. The MSBs can be programmed using the WROWS register.
4:3	WStart Row[1:0]	The two LSBs of the windows row start address are fixed to 0Hex. Although these bits can be written to they will have on effect on the LSBs of the window's row start address.
2	WEndRow[2]	Use to program the scan window's end row address's LSBs. The MSBs can be programmed using the WROWE register
1:0	WEnRow[1:0]	The two LSBs of the windows row end address are fixed to 3Hex. Although these bits can be written to they will have on effect on the LSBs of the window's row end address.

NOTE: The Row and Column start and end registers should be written to at power up to guarantee that the expected window size is set.

Register Name Active Window Column Start Register
Address 1C Hex
Mnemonic WCOLS
Type Read/Write (Double Buffered)
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	WStart-Col[10:3]	Use to program the display window's start column address' MSBs. The LSBs can be programmed using the WCOLLSB register.

Register Name Active Window Column End Register
Address 1D Hex
Mnemonic WCOLE
Type Read/Write (Double Buffered)
Reset Value 28 Hex.

Bit	Bit Symbol	Description
7:0	WEnd-Col[10:3]	Use to program the scan window's end column address' MSBs. The LSBs can be programmed using the WCOLLSB register.

Register Name Active Window Column LSB Register
Address 1E Hex
Mnemonic WCOLLSB
Type Read/Write (Double Buffered)
Reset Value 23 Hex.

Bit	Bit Symbol	Description
7:6		Reserved
5	WStartCol[2]	Use to program the display window's start column address' LSBs. The MSBs can be programmed using the WCOLS register.
4:3	WStart Col[1:0]	The two LSBs of the windows column start address are fixed to 0Hex. Although these bits can be written to they will have on effect on the LSBs of the window's column start address.
2	WEndCol[2]	Use to program the scan window's end column address' LSBs. The MSBs can be programmed using the WCOLE register.
1:0	WEndCol[1:0]	The two LSBs of the windows column end address are fixed to 3Hex. Although these bits can be written to they will have on effect on the LSBs of the window's column end address.

Register Set (continued)

Register Name Frame Delay High Register
Address 20 Hex
Mnemonic FDELAYH
Type Read/Write (Double Buffered)
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Fdelay[14:7]	Use to program the MSBs of the frame delay. Note the max allowed frame delay is 32767.

Register Name Frame Delay Low Register
Address 21 Hex
Mnemonic FDELAYL
Type Read/Write (Double Buffered)
Reset Value 08 Hex.

Bit	Bit Symbol	Description
7		Reserved.
6:0	Fdelay[6:0]	Use to program the LSBs of the frame delay. Note the max allowed frame delay is 32767.

Register Name Row Delay High Register
Address 22 Hex
Mnemonic RDELAYH
Type Read/Write (Double Buffered)
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Rdelay[12:5]	Use to program the MSBs of the row delay.

Register Name Row Delay Low Register
Address 23 Hex
Mnemonic RDELAYL
Type Read/Write (Double Buffered)
Reset Value 08 Hex.

Bit	Bit Symbol	Description
7:5		Reserved.
4:0	Rdelay[4:0]	Use to program the LSBs of the row delay.

Register Name Integration Time High Register
Address 24 Hex
Mnemonic ITIMEH
Type Read/Write (Double Buffered)
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:4		Reserved
3:0	Itime[10:7]	Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset. Itime can not be greater then the number of active rows.

Register Name Integration Time High Register
Address 25 Hex
Mnemonic ITIMEL
Type Read/Write (Double Buffered)
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7		Reserved.
6:0	Itime[6:0]	Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset.

Register Name Black Level Configuration Register
Address 40 Hex
Mnemonic BLKLEVCONFIG
Type Read/Write
Reset Value 07 Hex.

Bit	Bit Symbol	Description
7		Reserved.
3	$\overline{\text{BlkLevEn}}$	Set to a logic 1, (the default) to disable the internal black level compensation circuit. Set to a logic 0 to enable the internal black level compensation circuit.
2:0	BlkRate	Use to adjust the rate at which the auto black level circuit converges to the programmed target, *BlkTarget*. See section 7.3 for more information.

Register Name Reference Black Level Register
Address 41 Hex
Mnemonic BLKTARGET
Type Read/Write
Reset Value 10 Hex.

Bit	Bit Symbol	Description
7:0	BlkRef	Use to program the target black level. See section 7.3 for more information.

Register Set (continued)

Register Name PGA Channel 0 Register
Address 42 Hex
Mnemonic PGA0
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7		Reserved
6:0	PGA0	Use to program the analog gain of color channel 0. Max gain is 16dB of gain programmable in 128 steps of 0.125dB.

Register Name PGA Channel 1 Register
Address 43 Hex
Mnemonic PGA1
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7		Reserved
6:0	PGA1	Use to program the analog gain of color channel 1. Max gain is 16dB of gain programmable in 128 steps of 0.125dB.

Register Name PGA Channel 2 Register
Address 44 Hex
Mnemonic PGA2
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7		Reserved
6:0	PGA2	Use to program the analog gain of color channel 2. Max gain is 16dB of gain programmable in 128 steps of 0.125dB.

Register Name PGA Channel 3 Register
Address 45 Hex
Mnemonic PGA3
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7		Reserved
6:0	PGA3	Use to program the analog gain of color channel 3. Max gain is 16dB of gain programmable in 128 steps of 0.125dB.

Register Name Offset Channel 0 Register
Address 46 Hex
Mnemonic OFFSET0
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Offset0	Use to manually set the black level for gain channel 0. See section 7.2 for more information.

Register Name Offset Channel 1 Register
Address 47 Hex
Mnemonic OFFSET1
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Offset1	Use to manually set the black level for gain channel 1. See section 7.2 for more information.

Register Name Offset Channel 2 Register
Address 48 Hex
Mnemonic OFFFSET2
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Offset2	Use to manually set the black level for gain channel 2. See section 7.2 for more information.

Register Name Offset Channel 3 Register
Address 49 Hex
Mnemonic OFFSET3
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Offset3	Use to manually set the black level for gain channel 3. See section 7.2 for more information.

Register Name Gain Color Map Register
Address 4A Hex
Mnemonic CFAMAP
Type Read/Write
Reset Value 1B Hex.

Bit	Bit Symbol	Description
7:6	ColorMap0	Use to program the color map for gain channel 0. See section 6.2 for more information. **Note: When using monochrome sensor set all bits [7:0] to 0.**
5:4	ColorMap1	Use to program the color map for gain channel 1. See section 6.2 for more information.
3:2	ColorMap2	Use to program the color map for gain channel 2. See section 6.2 for more information.
1:0	ColorMap3	Use to program the color map for gain channel 3. See section 6.2 for more information.

Register Set (continued)

Register Name VSYNC Latency Register
Address 50 Hex
Mnemonic VSYCADJUST
Type Read/Write
Reset Value 08 Hex.

Bit	Bit Symbol	Description
7:6		Reserved.
4:0	VsyncEnd	By default, in pulse mode the **vsync** signal will remain active for four **pclk** periods after end of frame. In level mode **vsync** will remain active for the duration of the frame delay time. Use to adjust the time that the **vsync** signal goes inactive in multiples of **pclk** as follows: 0000 — no **vsync** pulse 00001 to 00111 — Reserved 01000 — no adjustment, the default 01001 to 11111 — +1 **pclk** clock to +24 **pclk** clocks

Register Name HSYNC Latency Register
Address 51 Hex
Mnemonic HSYNCADJUST
Type Read/Write
Reset Value 08 Hex.

Bit	Bit Symbol	Description
7:4		Reserved.
3:0	HsyncEnd	By default, in pulse mode the **hsync** signal will remain active for four **pclk** periods after end of each row. In level mode **hsync** will remain active for the duration of the row delay time. Use to adjust the time that the **hsync** signal goes inactive in multiples of **pclk** as follows: 0000 — no **hsync** pulse 0001 to 0111 — Reserved 01000 — no adjustment, the default 1001 to 1111 — +1 **pclk** clock to +8 **pclk** clocks

Register Name Synchronization Adjustment Register
Address 52 Hex
Mnemonic DVBUSCONFIG0
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:4	VsyncStart	By default, in pulse mode the **vsync** signal will remain active for four **pclk** periods after end of frame. In level mode **vsync** will remain active for the duration of the frame delay time. Use to adjust the time that the **vsync** signal goes active in multiples of **pclk** as follows: 0000 to 1111 — 0 **pclk** clocks to -15 **pclk** clock
3:0	HsyncStart	By default, in pulse mode the **hsync** signal will remain active for four **pclk** periods after end of row. In level mode **hsync** will remain active for the duration of the row delay time. Use to adjust the time that the **hsync** signal goes active in multiples of **pclk** as follows: 0000 to 1111 — 0 **pclk** clocks to -15 **pclk** clock

Register Set (continued)

Register Name Polarity Adjustment Register
Address 53 Hex
Mnemonic DVBUSCONFIG1
Type Read/Write
Reset Value 0C Hex.

Bit	Bit Symbol	Description
7		Reserved
6	PixClkMode	Set the to a logic 1 to operate **pclk** to “data ready mode”. Set to a logic 0, the default, to set **pclk** to “*free running mode*”.
5	VsyncMode	Set to a logic 1 to operate the **vsync** pin to “pulse mode”. Set to a logic 0, (the default) to operate the **vsync** signal to “level mode”.
4	HsyncMode	Set to a logic 1 to operate the **hsync** signal to pulse for a minimum of four pixel clocks at the end of each row. Set to a logic 0, (the default) to force the **hsync** signal to a level indicating valid data within a row.
3:2		Reserved
1	VsyncPol	Assert to force the **vsync** signal to generate a logic 1 during a frame readout *(Level Mode),* or a negative pulse at the end of a frame readout *(Pulse Mode)*. Clear (the default) to force the **vsync** signal to generate a logic 0 during a frame readout *(Level Mode),* or a positive pulse at the end of a frame readout *(Pulse Mode)*. **NOTE:** In slave mode this bit must be set to 0.
0	HsyncPol	Assert to force the **hsync** signal to generate a logic 1 during a row readout *(Level Mode),* or a negative pulse at the end of a row readout *(Pulse Mode)*. Clear (the default) to force the **hsync** signal to generate a logic 0 during a row readout *(Level Mode),* or a positive pulse at the end of a readout *(Pulse Mode)*. **NOTE:** In slave mode this bit must be set to 0.

Register Name Video Output Adjustment Register
Address 54 Hex
Mnemonic DVBUSCONFIG2
Type Read/Write
Reset Value F0 Hex.

Bit	Bit Symbol	Description
7	OutputEn	Set to a logic 0 to tri-state all output signals (data and control) on the digital video port. set to a logic 1, (the default) to enable all signals (data and control) on the digital video port.
6	BlkPixelEn	Set to a logic 1, (the default) to read out the middle 8 black pixels at the start of every row. Set to a logic 0 to mask out the black pixel readout. **NOTE:** In master mode when the black pixels are enabled the active edge of Hsync corresponds to the first black pixel.
5	PixClkPol	Set to a logic 1 to set the active edge of the pixel clock to negative. Set to a logic 1, (the default), to set the active edge of the clock to positive.
4		Reserved
3:0	Bshift[3:0]	Use to program the routing of the MSB output of the internal video A/D to a bit on the digital video bus.

0000	A/D[9:0] -> d[9:0]
0001	A/D[9:0] -> d[8:0],d[9]
0010	A/D [9:0] ->d[7:0],d[9:8]
0011	A/D [9:0] -> d[6:0],d[9:7]
0100	A/D [9:0] -> d[5:0],d[9:6]
0101	A/D[9:0] -> d[4:0],d[9:5]
0110	A/D [9:0] -> d[3:0],d[9:4]
0111	A/D [9:0] -> d[2:0],d[9:3]
1000	A/D [9:0] ->d[1:0],d[9:2]
1001	A/D [9:0] -> d[0],d[9:1]
1010	A/D [9:0] -> d[9:0]

Register Set (continued)

Register Name **Video Output Tristate Adjustment Register**
Address **55 Hex**
Mnemonic **DVBUSCONFIG3**
Type **Read/Write**
Reset Value **00 Hex.Register Set** (continued)

Bit	Bit Symbol	Description
7:5		Reserved
4	Tristate	Digital output tristate. Set this bit to 1 to tristate all digital outputs. (**vsync**, **hsync**, **pclk**, data, external sync). Use can override this setting with independent override bits.
3	VsOverride	Overrides tri-stating of Vsync port in master timing mode. To enable override, set bit to 1.
2	HsOverride	Overrides tri-stating of Hsync port in master timing mode. To enable override, set bit to 1.
1	PclkOverride	Overrides tri-stating of Pclk port in master timing mode. To enable override, set bit to 1.
0	ExtSyncOver-ride	Overrides tri-stating of external sync port in master timing mode. To enable override, set bit to 1.

Register Name **Initialization Register 1**
Address **80 Hex**
Mnemonic **INITREG1**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:0	PixCal	Write 5 Hex to enable the pixel offset calibration circuits. Notes: This register can only be accessed when the Int2 parameter in the INTREG2 register is set to 01Hex. PixCal should be reset to 00Hex at the end of the pixel offset calibration procedure (see section 7.1 for more details).

Register Name **Pixel Offset Register**
Address **83 Hex**
Mnemonic **PIXELOFFSET**
Type **Read/Write**
Reset Value **1E Hex.**

Bit	Bit Symbol	Description
7:0	PixelOffset	Use to compensate for the sensors natural pixel offset. See section 7.1 for more details.

Register Name **Power Down Control Register**
Address **85 Hex**
Mnemonic **POWCTRL**
Type **Read/Write**
Reset Value **81 Hex.**

Bit	Bit Symbol	Description
7:0	Patrol	Write 82Hex before power down to minimize the sensor's power down current. Write 81Hex after power up from the power down mode to ensure correct operation of the sensor. Refer to section 9.2 for more information.

Register Name **Initialization Register 2**
Address **88 Hex**
Mnemonic **INITREG2**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:0	Int2	Write 1 Hex to activate the sensor's initialization registers Write 0 Hex to disable the sensor's initialization registers. Note this register is used for • the pixel array offset calibration (section 7.2) • power/up and down of the array (section 8.2)

Timing Information

1.0 DIGITAL VIDEO PORT MASTER MODE TIMING LEVEL MODE

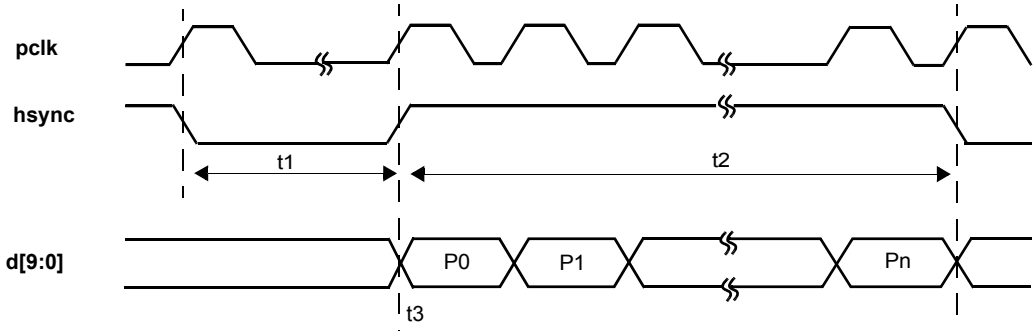


Figure 45. Row Timing Diagram

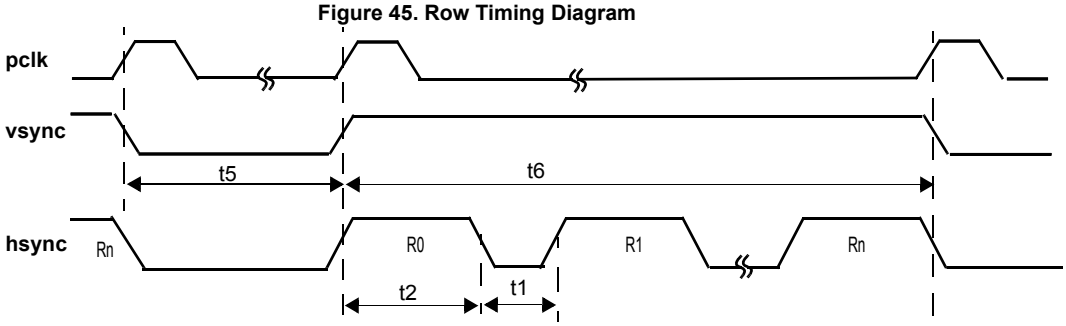


Figure 46. Frame Timing

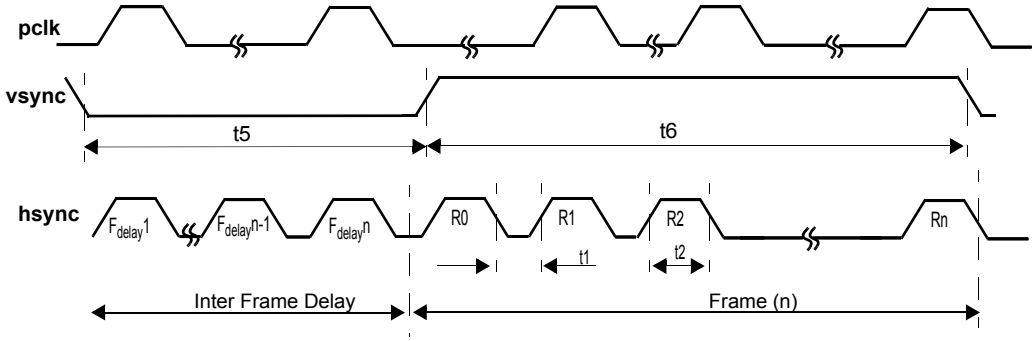


Figure 47. Frame Delay Timing (With Inter Frame Delay).

Label	Descriptions	Min	Typ	Max
t0	**pclk** period	37.04ns	45.45ns	83.33ns

t1	**hsync** inactive[1,2] level mode	(RN_{Hclk} - N_{pix} + *HsyncStart* - *HsyncEnd* - *8*BlkPixelEn*) * Hclk
t2	**hsync** active[1,2] level mode	(*HsyncEnd* - *HsyncStart* + *8*BlkPixelEn* + N_{pix}) * Hclk
t3	first valid pixel data after **hsync** active	*HsyncStart* * *Hclk*
t5	**vsync** inactive[1,3] level mode	((F_{delay} **RN_{Hclk}*) + $R_{opcycle}$ + R_{itime} + *VsyncStart* - *VsyncEnd*) * Hclk
t6	**vsync** active[1,3] level mode	(*VsyncEnd* - *VsyncStart* + (RN_{Hclk} * N_{rows})) * Hclk

1. See section 6.4 for definitions of RN_{Hclk} and FN_{Hclk}
2. The values of *HsyncStart* and *HsyncEnd* are stored in the DVBUSCONFIG0 and HSYNCADJUST registers respectively.
3. The values of *VsyncStart* and *VsyncEnd* are stored in the DVBUSCONFIG0 and VSYNCADJUST registers eruptively.

Timing Information

2.0 DIGITAL VIDEO PORT MASTER MODE TIMING PULSE MODE

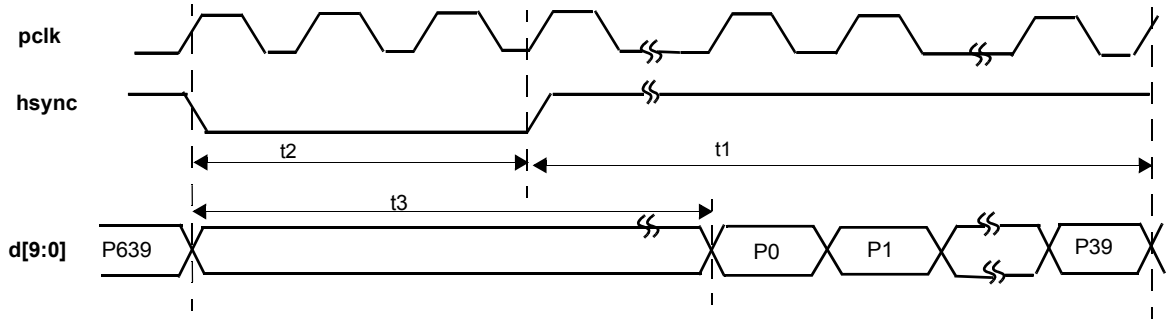


Figure 48. Row Timing Diagram

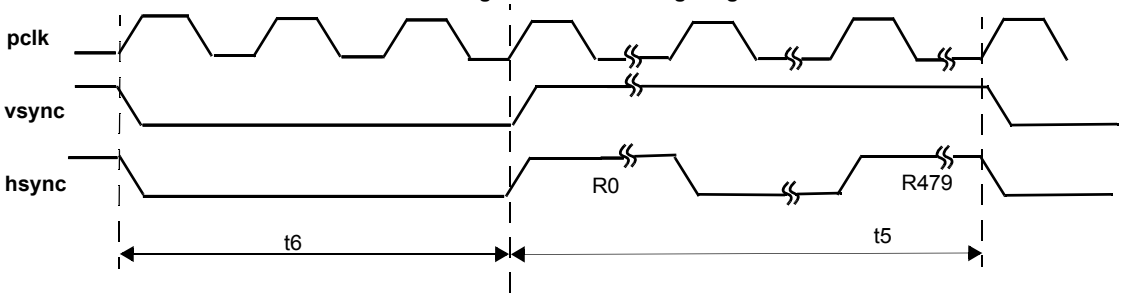


Figure 49. Frame Timing

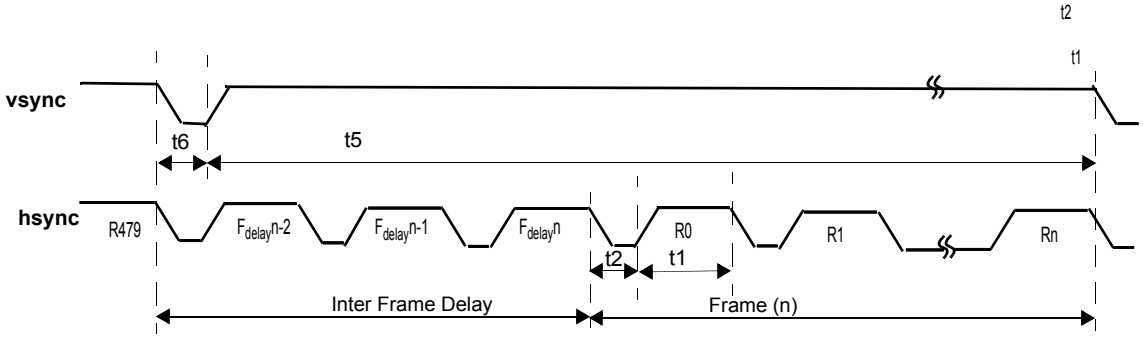


Figure 50. Frame Delay Timing (With Inter Frame Delay).

Label	Descriptions	Min	Typ	Max
t0	**pclk** period	37.04ns	45.45ns	83.33ns

t1	**hsync** inactive[1,2]	pulse mode	(RN_{Hclk} - *3)* * Hclk
t2	**hsync** active[1,2]	pulse mode	*3* * Hclk
t3	first valid pixel data after **hsync** active		*145 * Hclk*
t5	**vsync** inactive[1,3]	pulse mode	(FN_{Hclk} - *3)* * Hclk
t6	**vsync** active[1,3]	pulse mode	*3* * Hclk

1. See section 6.4 for definitions of RN_{Hclk} and FN_{Hclk}
2. The values of *HsyncStart* and *HsyncEnd* are stored in the DVBUSCONFIG0 and HSYNCADJUST registers respectively.
3. The values of *VsyncStart* and *VsyncEnd* are stored in the DVBUSCONFIG0 and VSYNCADJUST registers eruptively.

Timing Information (continued)

3.0 DIGITAL VIDEO PORT SLAVE MODE TIMING

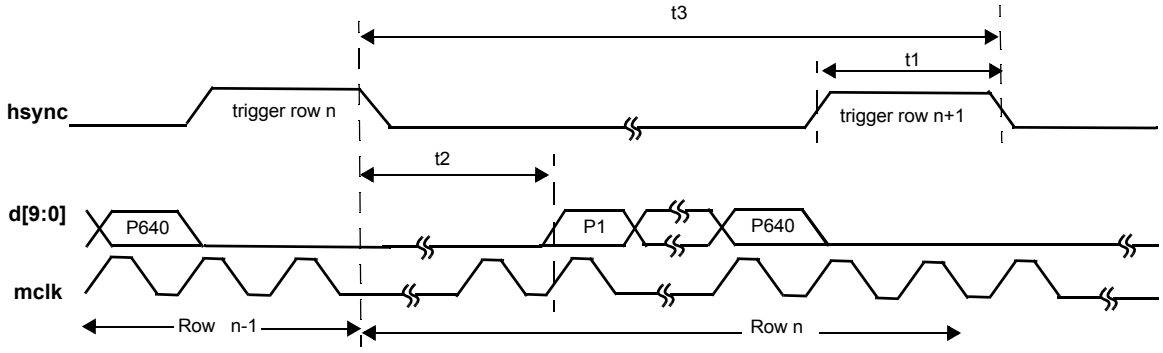


Figure 51. Slave Mode Row Trigger and Readout Timing

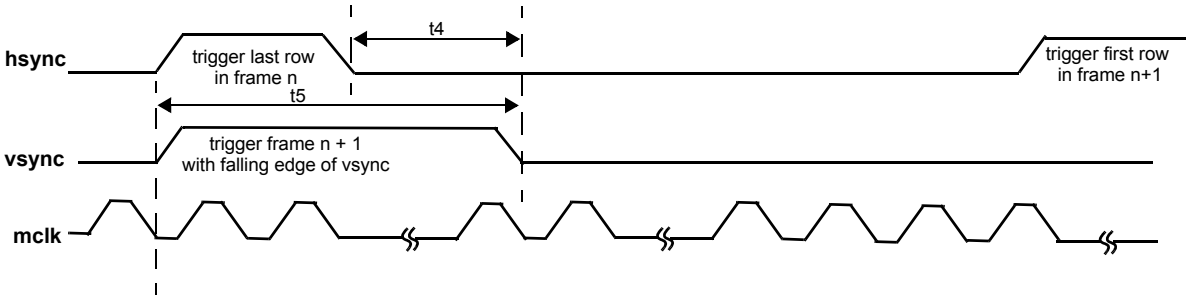


Figure 52. Slave Mode d[9:0], hsync & vsync to pclk Timing

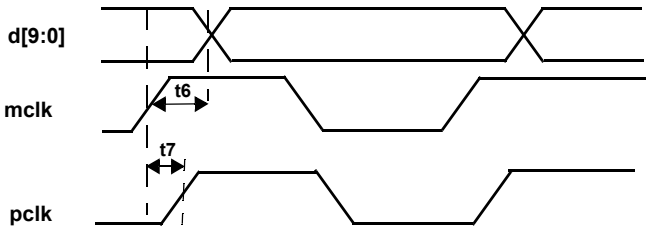


Figure 53. Rising Edge of mclk to Valid Pixel Data

The following specifications are from simulation. For the minimum value the conditions are all supply pins = +3.0V & C_L = 5pF and 0C while the maximum value conditions are all supply pins = 3.6V & C_L = 25pF.

Label	Descriptions	Min	Typ	Max
t1	Pulse width of row trigger	2 * **mclk**		
t2	First pixel out after falling edge of row trigger[1]	X_{mclk}	X_{mclk}	X_{mclk}
t3	Minimum time between row triggers[2]	(X_{mclk} +N_{col}) * **mclk**		
t4	Time to falling edge of frame trigger after falling edge of last row trigger in current frame.	1***mclk**		96 * **mclk**
t5	Pulse width of Frame trigger	3***mclk**		
t6	Time to valid pixel data after rising edge of **mclk**	14.9ns		39.7ns
t7	Time to **pclk** rising edge after rising edge of **mclk**	14.5ns		35.0ns

1. See section 10.6 for definition of X_{mclk}

Timing Information (continued)

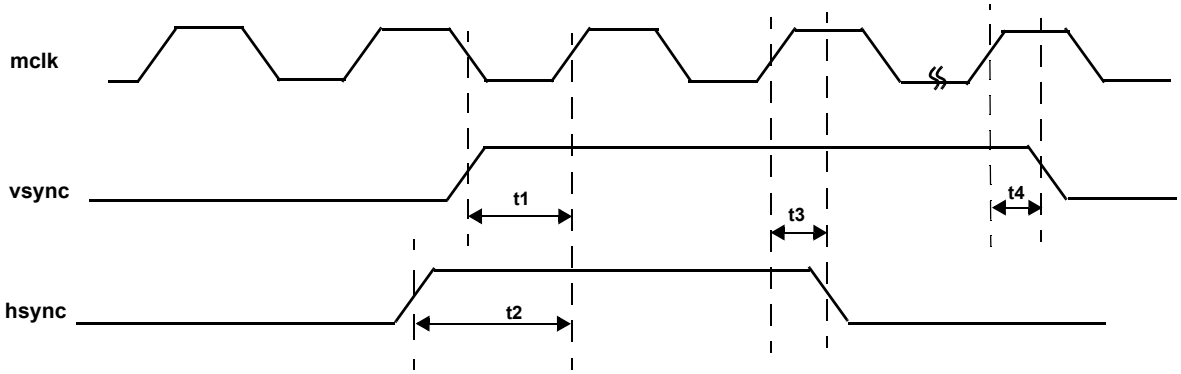


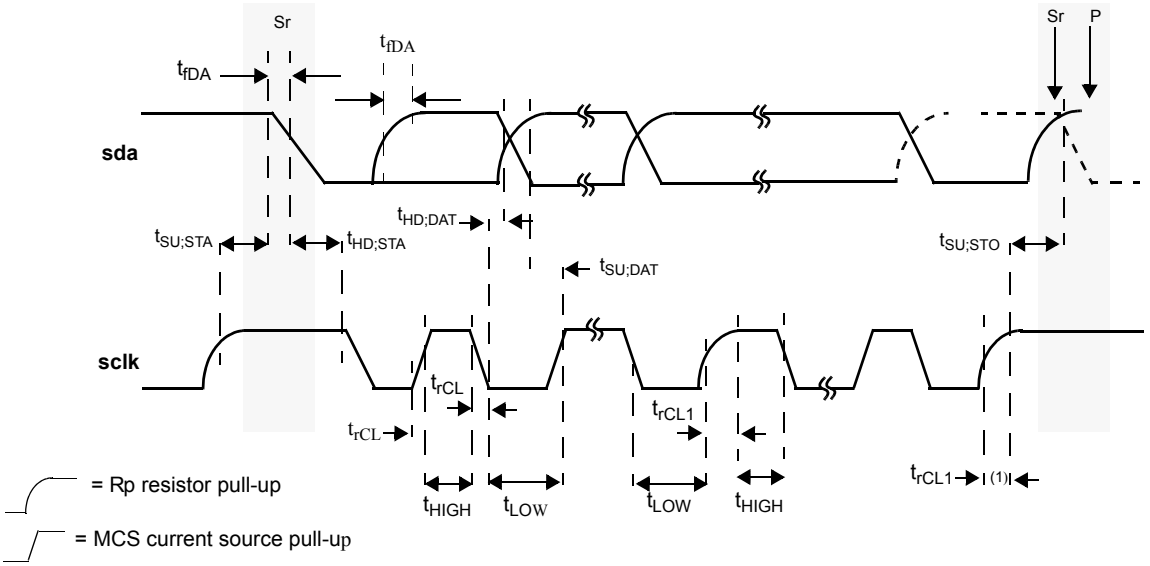
Figure 54. Set up and Hold Times for Slave Mode

PARAMETER	LABEL	MIN	MAX	UNIT
Vsync rising edge to Mclk rising (set-up time)	t1	-6.0	14.6	ns
Hsync rising edge to Mclk rising (set-up time)	t2	-7.3	14.2	ns
Mclk rising edge to Hsync falling edge (hold time)	t3	23.8	45.3	ns
Mclk rising edge to Vsync falling edge (hold time)	t4	23.4	44.0	ns

Figure 55. Set up and Hold times for Slave Mode

Timing Information (continued)

1.0 SERIAL BUS TIMING



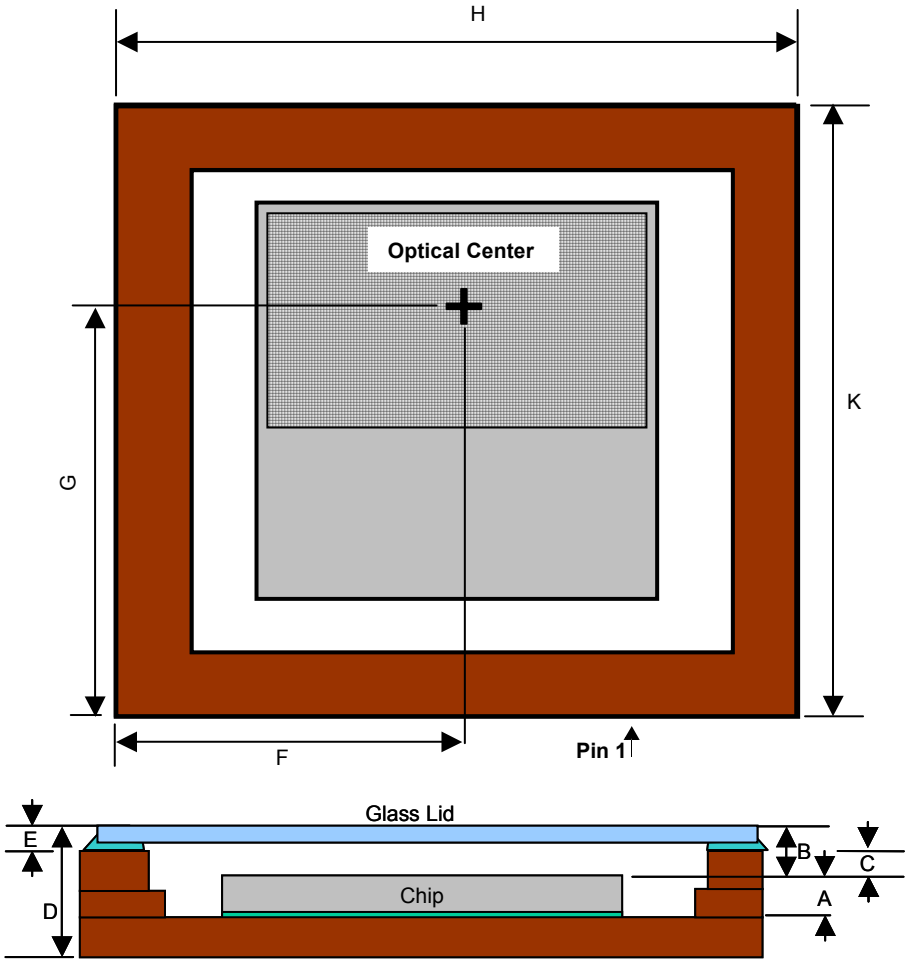
(1) Rising edge of the first **sclk** pulse after an acknowledge bit.

Figure 1. I²C Compatible Serial Bus Timing.

The following specifications apply for all supply pins = +3.3V, C_L = 10pF, and *sclk* = 400KHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

PARAMETER	SYMBOL	MIN	MAX	UNIT
sclk clock frequency	f_{SCLH}	0	400	KHz
Set-up time (repeated) START condition	$t_{SU;STA}$	0.6	-	µS
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	-	µS
LOW period of the **sclk** clock	t_{LOW}	1.3	-	µS
HIGH period of the **sclk** clock	t_{HIGH}	0.6	-	µS
Data set-up time	$t_{SU;DAT}$	180	-	nS
Data hold time	$t_{HD;DAT}$	0	0.9	µS
Set-up time for STOP condition	$t_{SU;STO}$	0.6		µS
Capacitive load for and **sclk** lines	C_b		400	pF

Mechanical Information



Dimension	Description	min (mm)	typ (mm)	max (mm)
A	Distance from top of die to bottom of cavity	0.788	0.820	0.852
B	Top of die to top of glass lid	0.690	0.970	1.250
C	Top of package to bottom of glass lid	0.250	0.420	0.590
D	Max total thickness of package			2.580
E	Thickness of lid	0.530	0.640	0.750
F	X-Coordinate of optical center (nom)		5.340	
G	Y-Coordinate of optical center (nom)		6.425	
H	X-Dimension of Package	10.540	10.670	10.970
K	Y-Dimension of Package	10.540	10.670	10.970
	Die Rotational Accuracy	-2^o	0^o	$+2^o$

Package Information